Stretchable Si Logic Devices with Graphene Interconnects

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Stretchable electronics have led to promising classes of electronic device applications such as tactile sensors for artificial electronic skins,[1–4] wearable electronic devices,[5,6] stretchable displays,[7–11] logic devices,[12,13] and electronic circuits.[14,15] In the stretchable forms of electronic circuits, interconnects have the important role in assigning the stretchability of circuits. A variety of materials, including organic, carbon-based, metal nanowire-shaped, and hybrid conductors have been studied as potential stretchable interconnects.[16–20] Although these materials remain conductive even under high strain, the difficulties related to fine patterning via conventional lithography and poor reproducibility and performance have limited their integration with inorganic materials for high-performance devices. An alternative method, which could avoid this limitation, would be to use graphene as the stretchable interconnect material. Graphene is suited for this task because it offers good electrical and mechanical properties. Moreover, it is compatible with conventional lithographic methods such as photolithography and dry plasma etching, enabling scalable integration to the Si-based electronics.[21–27] Although some research has been conducted to confirm the possibility of using graphene as an interconnect for rigid Si integrated circuits,[28–30] there are still significant challenges in applying graphene to stretchable electronic systems.

In this work, we demonstrated these concepts through electrical characterization and mechanical analysis of stretchable Si logic devices combined with graphene interconnects. The resulting devices exhibited good electrical properties and stable mechanical performance without serious device degradation under high external strain. The failure strain of polycrystalline graphene grown by chemical vapor deposition (CVD) is known to be relatively low compared to that of defect-free, monolayer graphene due to unavoidable defects such as grain boundaries, contaminants, and microcracks that are generated from the growth, etching, and transfer processes.[31–34] To improve the limited stretching range and the weak electrical conductivity of monolayer graphene, multilayer stacked graphene was used; stacked layers can cover the defects of each individual layer and enable layers to slide over each other.[35]

Figure 1 shows the mechanical and electrical properties of the graphene interconnects connected with Si plates on a polydimethylsiloxane (PDMS) substrate before the fabrication of real devices. Ribbon-shaped graphene interconnects were designed to reduce the total stiffness of the interconnects because the applied strain is concentrated on the interconnect region (with low stiffness) instead of on the rigid active device region.[36] Graphene has the advantage of reduced stiffness due to its ultrathin atomic thickness, although it does have a very high elastic modulus (≈1 TPa).[23,33] The stiffness of the Si regions and graphene interconnects on PDMS were calculated with Equation (1)

$$K = \frac{P}{\delta} = \sum_i E_i \frac{A_i}{L_i} \,[\mathrm{N\ m^{-1}}], \tag{1}$$

where K is the stiffness of the stacked film, P is the load, δ is the change in length, E is the elastic modulus, A is the cross-sectional area, L is the length of the film, and i is the layer index. The ribbon-shaped graphene interconnect, which has long length and narrow width, produces the low stiffness following the Equation (1). However, the resistance of the graphene interconnects is inversely proportional to the ratio of the width to the length. Thus, there is a trade-off relationship between the resistance and the stiffness of the graphene. Considering the two factors, the graphene interconnect was designed as the length of 550 μm and the width of 100 μm. (Figure 1a). The calculated stiffness values of the graphene/Si plate and the graphene interconnect are ≈24400 N m^{-1} and ≈648 N m^{-1}, respectively. Therefore, it is expected that most of the strain will be concentrated in the interconnect region (with the lower stiffness). As a result, when the substrate was stretched to 5% and 12%, the lengths of the interconnects increased to 581.2 and 626.4 μm, respectively, corresponding to length increments of 7.6% and 16%. In contrast, the length of Si was hardly changed because most of the external strain is concentrated on the graphene interconnect, which has lower stiffness. The summation of the deformation in each region corresponded well to the total deformation of the substrate, as shown in Figure 1a, which suggests that the measurement of the strain distribution in each region is reliable.

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DOI: 10.1002/smll.201502338

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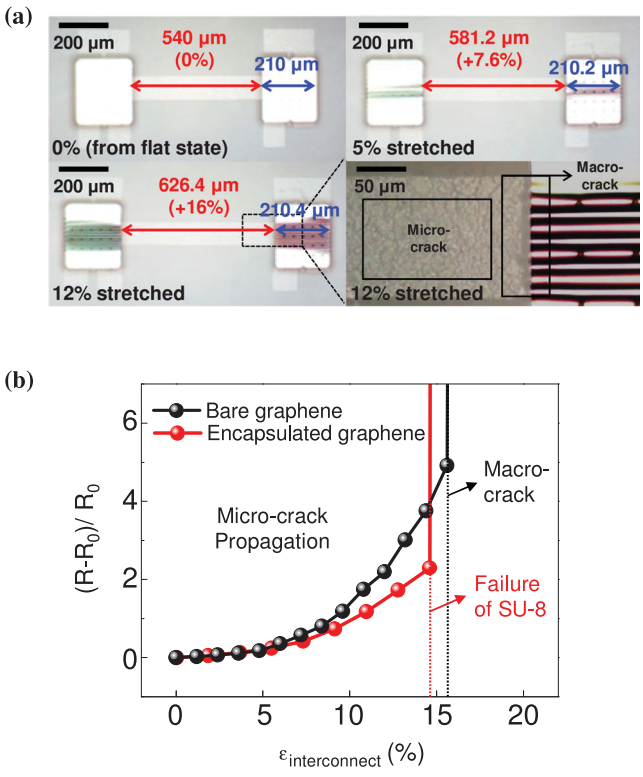

Figure 1. Electrical and mechanical properties of graphene interconnects. a) Optical microscope images of a graphene ribbon on a patterned Si plates at different stretching levels (0%–12%), and a magnified image of the edge of Si at a 12% stretched state. b) Normalized variation of the resistance according to the strain level applied to the interconnect in bare graphene and encapsulated graphene.

Figure 1b presents the change in the resistance of multilayer graphene (≈10 layers) with respect to the tensile strain. The resistance change can be divided into two regions, which show gradual and rapid increases in the resistance. Such distinct changes in the resistance of graphene interconnects can be explained by two failure mechanisms in the graphene: microcrack propagation and macrocrack generation. At tensile strains less than 15.6%, a gradual increase in the resistance is observed. This phenomenon can be explained by the generation and propagation of microcracks.[37,38] The low density of cracks and pinholes in graphene, which resulted from the CVD synthesis, etching, and transfer processes, induces the propagation of these microcracks in graphene.[33,34] This leads to a gradual increase in the resistance during the stretching test.[35] To compensate for the propagation of microcracks, polymer encapsulation (SU-8, $K_{SU\text{-}8}$ ≈1800 N m^{-1}) was used. This encapsulation alleviates the stress concentration on the cracked parts and delays crack propagation during mechanical stretching because SU-8 has a higher stiffness than PDMS (K_{PDMS} ≈333 N m^{-1}) and graphene (K_{grp} ≈648 N m^{-1}).[39,40] Alternatively, a severe increase in the resistance was induced by the formation of macrocracks, which can be observed by an optical microscope, at a strain of 15.6%. The creation of macrocracks started at the edge between graphene and the Si plate; this was caused by the large height difference between the Si plate and graphene as well as the shape of the edge, which induced stress concentration effects.

To confirm the function of graphene interconnects in actual Si integrated circuits, we fabricated n-channel metal oxide semiconductor Si inverter arrays on rubber substrates. Two thin film transistors (TFTs) with different channel lengths (to compensate for the current value) were formed on an SU-8/SiO_2/Ge substrate as shown in **Figure 2**a. The source and drain regions were highly n-doped (>10^{20} cm^{-3}) to produce tunneling-based ohmic contact with the graphene electrodes. In contrast to conventional metal electrodes deposited by evaporation, atomically thin graphene can be partially suspended on 1–2 nm thick native oxides that are formed on the Si surface; this can seriously increase the contact resistance due to interrupted physical contact. To solve this problem, few-nanometer-thick Au nanoparticles (NPs) were deposited on the contact area to improve physical contact between the two materials.[41,42] The TFT arrays were transferred to a PDMS substrate that was isotropically prestretched as much as 5%, and attempts were made to enhance the stretchability through selective etching and dry transfer processes (Figure 2b–d). Interestingly, most of the applied prestrain was concentrated on the graphene interconnect, resulting in the formation of a wavy geometry; conversely, rigid Si TFTs were flat without a wavy structure.[43,44]

In contrast to the stretchable graphene interconnect, the active materials are significantly broken by small amounts of strain because these parts consist of brittle inorganic materials such as Si and SiO_2 (failure strains of ≈0.8% and 0.57%, respectively).[45,46] The electrical performances of inverter arrays were characterized with respect to tensile strains up to 10% (Figure 2e). The stretching modes are divided into two stages: prestrained (0%–5%) and post-strained (5%–10%) stages. In the first stage, a prestrain of 5%, stored in the wavy interconnects, was gradually consumed by an applied strain. The height of the wrinkles was observed to decrease from 7.5 to 0 μm (Figure 2f). In the second stage, the tensile strain continuously focused on the interconnect (with low stiffness) and broke the interconnect at a strain of 11%. To carefully evaluate the tensile strain applied at the interconnect, the local deformation was observed with an optical microscope (Figure 2g). The graphene interconnect should be significantly stretched because the Si TFT island region was barely changed by the applied tensile strain. The interspace between islands were stretched as 7.0% and 11.9% when the substrate felt stretching levels of 5% and 10%, respectively. The intersection of the bridge and the island was disconnected by high local strain at a stretching levels of 11%. In addition, it was observed that in this tensile strain range, vertical compressive strain caused by the Poisson effect of the PDMS substrate has a negligible influence on the active Si device area (Figure S4, Supporting Information).

Strain distributions around the active and the interconnect regions were calculated using finite element analysis (FEM). All layers in the device are modeled as shell elements with dissimilar materials properties because their thicknesses are very small compared with their lateral dimensions. It was assumed that the layers were tightly bonded with one another and partial sliding was generated at the interfaces between SU-8 and PDMS. The structure shown in Figure 2d has the

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DOI: 10.1002/smll.201502338

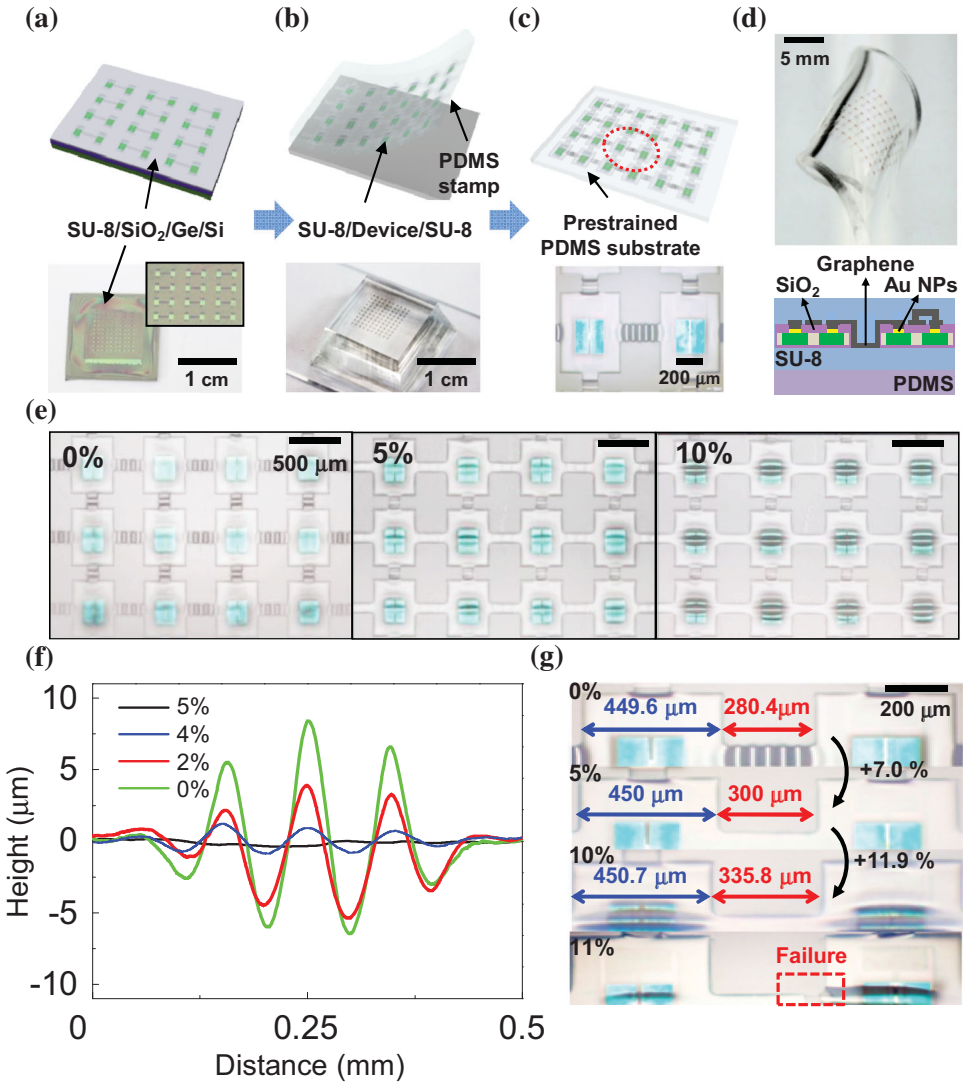

Figure 2. Schematic illustrations and optical images corresponding to the main fabrication steps for stretchable Si inverter arrays on rubbers using polymer encapsulated graphene interconnects. The frames correspond to the status after a) formation of devices on a wafer, b) delamination of them using a PDMS stamp, c) transfer onto prestrained PDMS substrates. d) An optical image of the stretchable inverters on a twisted PDMS substrate; the inset shows a vertical schematic layout of the inverter architecture, which connects two Si TFTs using a graphene interconnect. e) Optical microscope image of the array of six inverters with strains of 0%, 5%, and 10%. f) Height profiles of wavy interconnects during 5% stretching. g) Optical microscope image of the device with strains of 0%, 5%, and 10%, which shows that the distances between TFTs are 280.4 μm, 300 μm, and 335.8 μm, respectively. These values correspond to stretching of 7.0% and 11.9% when devices are stretched from 0% to 5% and from 5% to 10%, respectively.

same stacking order with that of actual device. Thickness and material properties for the FEM simulation were given in the Table S1 (Supporting Information). A quarter model was adopted considering the symmetries with respect to x and y axes. The tensile strain of 10% was applied as the boundary condition on the edges of PDMS and epoxy layers considering the experimental conditions. The distribution of normal strain in the tensile direction is displayed as **Figure 3**a where the interspace experiences large strain of 11% compared to the upper part of island of 0.7%. Locally concentrated strain of 10% was clearly observed at the intersection which corresponds to failure region in Figure 2g. Especially, the central region of graphene interconnect was under the strain of 7.2% as shown in Figure 3b. On the other hand, the maximum strain concentrated on Si and SiO_2 was less than 0.49% which is lower than the failure tensile strain of Si (≈0.8%) and and SiO_2 (≈0.57%).

Figure 4a,b displays the transfer and I_D–V_G characteristics before and after stretching of the TFTs inverters. Each TFT, composed of a single-crystal Si channel, exhibited an electron mobility of 210 ± 20 $cm^2\ V^{-1}\ s$, on/off ratio of ≈10^4, threshold voltage of 2.75 ± 0.25 V, and subthreshold swing of 0.62 V/decade in the unstretched state. The high-performances of the devices were achieved from the improvement of contact resistances by employing the Au NPs (Figure S5, Supporting Information). Because the Au NPs prevent the native oxide formation,[42] the contact resistance results from the two interfaces; the highly doped Si (10^{20} cm^{-3})/Au NPs interface and the Au NPs/graphene interface. The ohmic contact is achieved at the interface between the highly

DOI: 10.1002/smll.201502338

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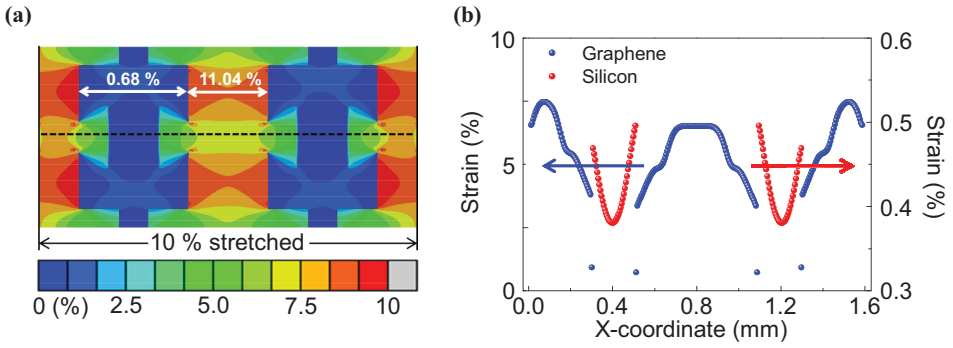

Figure 3. Analysis of strain distribution on the stretchable Si inverters on a PDMS by FEM. a) A simulated distribution of the strain, including two Si layers, SiO_2 thin films, and graphene interconnects. This shows that most of the total strain is placed on the graphene interconnect while negligible strain occurs in the active layer. b) Side views of the simulated strain distribution showing exact strain values in the graphene interconnect region and the silicon active layer region along the dash line.

doped Si/Au NPs by tunneling mechanism. In addition, the low contact resistivity of ≈550 Ω μm between Au and graphene has been reported.[47] In consequence, the negligible contact resistance in the device is created regardless of their sizes and the coverage rates (Figure S6, Supporting Information). The clear conducting path through the highly doped Si, Au NPs and graphene electrode generated very narrow hysteresis characteristics of the drain current with the hysteresis window of 0.37 V due to charge trapping in the NPs (Figure S7, Supporting Information). The high-performance of the devices was maintained, even after being stretched by 10%, without serious device degradation. In addition, the output characteristics and gain profiles of the inverter, which consists of two TFTs and graphene interconnects, exhibited stable operation within 20% of the electrical properties under stretching (Figure 4c). The voltage gain was as high as 2.07 ± 0.11 V and the threshold voltage (V_M) was 4 ± 0.22 V. The electrical properties of the inverters on rubber substrates were similar to that of the inverters on the SiO_2/Si wafer. However, small variations with reduction of noise margin and gain value are observed. This variation resulted from the detrimental effects such as the trapped ion charges existing at the interface between the Si channel and the rubber (Figure S8, Supporting Information). Moreover, these values

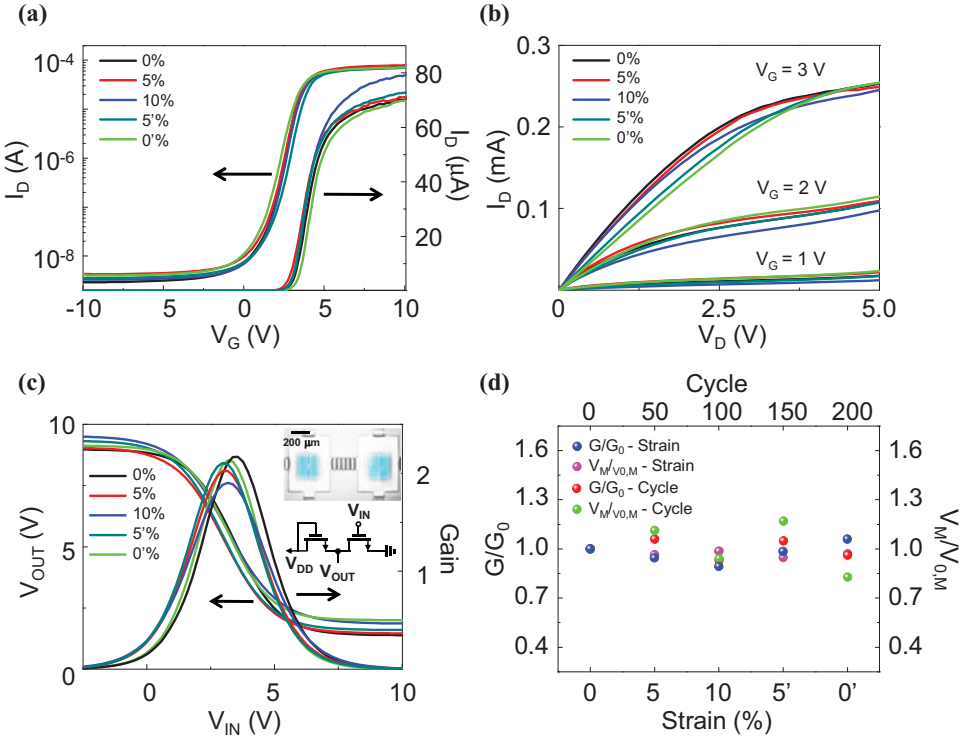

Figure 4. Electrical and mechanical properties of a constituent TFT and an inverter device under stretching (0%, 5%, and 10%) and recovery (5′% and 0′%). a) Transfer characteristics of devices on a PDMS substrate with stretching up to 10% on linear and log scales. The channel width and length of the device are 250 μm and 10 μm, respectively, with a V_D of 0.5 V. b) Current–voltage characteristics of the device biased with various gate voltages between 1 V (bottom) and 3 V (top) with a step size of 1 V. c) V_{OUT}–V_{IN} characteristics of the inverter biased with a V_{DD} of 10 V. Inset shows the device geometry. d) Normalized gain and V_M values in the initial, stretched, recovered, and cycled states.

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DOI: 10.1002/smll.201502338

for the inverters exhibited small irregular variations within 20%, even after repeated stretching of the substrate over 200 times (Figure 4d). These results indicate that the applied strain is well managed by the graphene interconnects and is not transferred to the brittle regions of the active devices.

In summary, we demonstrated stretchable Si-based logic devices that used multilayer graphene grown by CVD as the interconnects. The poor contact resistance between graphene and Si, caused by the rapid growth of native oxides on the Si surface, was resolved by the insertion of Au NPs, which lead to improved electrical contact between the two surfaces. The logic gates were integrated on a rubber substrate and displayed reliable electrical properties; this reliability was caused by a reduction of the actual strain applied to the active devices due to the presence of the graphene interconnects. This type of fabrication, combined with designs that concentrate the strain near the interconnects, provides a realistic path for the fabrication of circuits that require good mechanical stretchability.

Experimental Section

Fabrication of Stretchable Si Logic Device with Graphene Interconnects: First, the top Si layer (300 nm) of a silicon-on-insulator wafer was transferred onto an epoxy/SiO_2/Ge wafer, after elimination of the underlying SiO_2 layer. An SiO_2 dielectric layer (≈120 nm) was then grown by plasma enhanced chemical vapor deposition (PECVD). Next, Au NPs with thickness of 1, 2, and 3 nm were deposited by a thermal evaporator to decrease the contact resistance between Si and graphene. The Au NPs were aggregated in the form of discrete disks with average lateral diameter of 10, 15, and 20 nm, resulting in the coverage of 30%, 50%, and 70%, respectively (Figure S6, Supporting Information).[48] Multilayer graphene, which was grown by CVD with Ni catalysts with thickness of 300 nm, was transferred through previously reported procedures.[49,50] The graphene was patterned by conventional photolithography using AZ5214 as a photoresist (PR). To reduce the PR residue on the graphene, oxygen plasma through reactive ion etcher was treated to etch the graphene for a short time (≈5 s). Specific information about graphene is exhibited in Figures S1–S3 (Supporting Information). The top and bottom encapsulating epoxy layers (SU-8) were coated and defined to form a structure of islands and bridges. This structure was detached from the carrier wafer by removing a Ge sacrificial layer and transferred onto a stretchable PDMS. The arrays on the PDMS stamp were transfer-printed again onto a rubber substrate, which was prestretched as much as 5%, through a high-temperature process at 250 °C.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

W.L. and H.J. contributed equally to this work. This work was supported by the Global Frontier Research Center for Advanced Soft Electronics (2014M3A6A5060933) through the National Research Foundation of Korea (NRF), funded by the Ministry of Education, Science and Technology and the Research Program of Korea Institute of Machinery & Materials (SC 1090).

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Received: August 5, 2015
Revised: September 7, 2015
Published online:

DOI: 10.1002/smll.201502338