Vertical field effect tunneling transistor based on graphene-ultrathin Si nanomembrane heterostructures

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Vertical field effect tunneling transistor based on graphene-ultrathin Si nanomembrane heterostructures

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Abstract

Graphene-based heterostructured vertical transistors have attracted a great deal of research interest. Herein we propose a Si-based technology platform for creating graphene/ultrathin semiconductor/metal (GSM) junctions, which can be applied to large-scale and low-power electronics compatible with a variety of substrates. We fabricated graphene/Si nanomembrane (NM)/metal vertical heterostructures by using a dry transfer technique to transfer Si NMs onto chemical vapor deposition-grown graphene layers. The resulting van der Waals interfaces between graphene and p-Si NMs exhibited nearly ideal Schottky barrier behavior. Due to the low density of states of graphene, the graphene/Si NM Schottky barrier height can be modulated by modulating the band profile in the channel region, yielding well-defined current modulation. We obtained a maximum current on/off ratio (I_{on}/I_{off}) of up to $\sim 10^3$, with a current density of 10^2 A cm^{-2}. We also observed significant dependence of Schottky barrier height $\Delta\varphi_b$ on the thickness of the Si NMs. We confirmed that the transport in these devices is dominated by the effects of the graphene/Si NM Schottky barrier.

1. Introduction

Recent rapid progress in basic science and applications of graphene has opened the way for materials just one atom thick to be used in future electronics, including devices with new structures. Graphene's unique physical properties, such as its two-dimensional structure, high carrier mobility, and low density of states, make it attractive for high-speed electronic devices [1–5]. However, graphene-based field-effect transistors cannot be completely switched off due to the lack of an intrinsic band gap in graphene; hence, they are inappropriate for digital logic applications [6, 7]. On the other hand, heterostructures based on graphene and other two-dimensional crystals have been demonstrated that can be assembled into three-dimensional stacks with atomic-layer precision; these have shown a variety of fascinating physical phenomena and have aroused immense interest in demonstrating a prototype field-effect tunneling transistor, which is regarded as a candidate technology to replace complementary metal-oxide semiconductor technology [6, 8, 9]. In particular, various vertically layered heterostructures based on work function tunability of graphene have been studied recently, such as graphene-based tunneling transistors (called barristors) and vertical field-effect transistors (VFETs); these have shown improved I_{on}/I_{off} characteristics compared to planar graphene field-effect devices [10, 11]. The demonstration of such vertically stacked heterostructures has opened up potential high-performance applications in tunneling transistors, photovoltaic cells, and flexible devices based on two-dimensional (2D) materials. A broad range of possible materials can be incorporated into such stacks by weak van der Waals forces to create novel highly tailored heterostructures [3, 15, 16]. To create VFET heterojunctions, various kinds of 2D barrier materials have been considered, such as exfoliated hexagonal boron nitride, molybdenum disulfide, and tungsten disulfide, but critical challenges still remain for wafer-scale integration [12, 13, 17].

On the other hand, single-crystal Si NMs, formed in large sheets with precisely defined thicknesses comparable to 2D materials, offer unique advantages over other transition-metal dichalcogenides. Si NMs are compatible with established semiconductor techniques, and can have exceptional material quality, compositional purity, and high uniformity, leading to

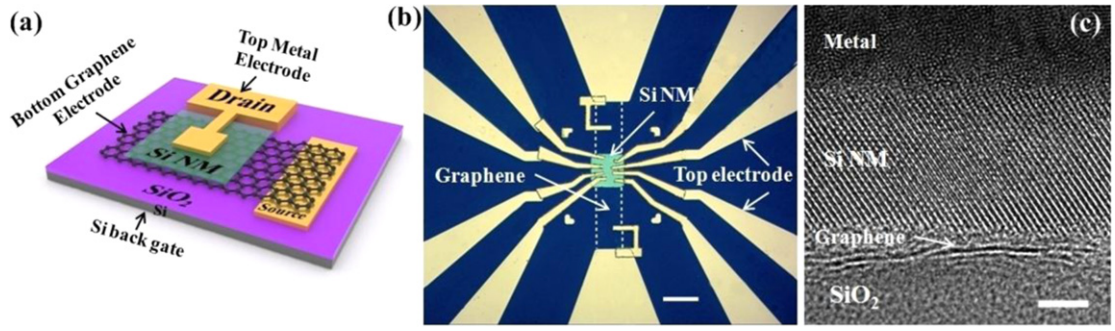

Figure 1. Graphene/Si NM heterostructure layout: (a) Three-dimensional schematic illustration of the vertically stacked graphene/Si NM/metal transistor. (b) Optical image of a typical vertical transistor device (scale bar: 40 μm). (c) Cross-sectional TEM image of a vertical transistor (scale bar: 2 nm).

straightforward paths for wide-scale integration into existing Si-based technology platforms. Transferrable single-crystal Si NMs are often more suitable than other 2D materials for use as active materials in flexible electronics due to their material uniformity, mechanical flexibility and durability, electrical properties equivalent to their bulk counterparts, easy handling and processing, and low cost [18–22]. There is a broad range of electronics applications in which mechanically flexible materials with higher speed are needed; these applications include flexible electronics and optoelectronics, including transparent electronics. Because the thickness of Si NMs is controllable, their use may allow this range of applications to be extended.

Herein we describe a new generation of vertical tunneling transistors in which ultrathin Si NMs serve as an ultrathin 2D barrier material between chemical vapor deposition (CVD)-grown graphene and a metal electrode. By utilizing the Schottky barrier height between graphene and Si NMs in ultrathin Si-based tunneling transistors, the device characteristics can be improved considerably, to the extent that the resulting device can satisfy the requirements for next-generation electronic devices. Ultrathin Si NMs offer distinct advantages over other 2D materials, including their chemical stability and moderate band gaps. Additionally, the use of the dry transfer technique with Si NMs can produce a clean interface between graphene and Si NMs that exhibits nearly ideal Schottky diode behavior, thereby yielding strong current rectification.

2. Experimental methods

Figure 1(a) schematically illustrates a typical vertical transistor of our design. The fabrication techniques for the vertical transistor are schematically illustrated in the methods section. Briefly, monolayer graphene was first grown by CVD and transferred onto a silicon wafer with a SiO_2 layer 285 nm thick [23]. Then, the transferred graphene layer was patterned by photolithography and oxygen plasma etching into strips 25 μm wide and 100 μm long to define the drain electrode. Si NMs of various thicknesses were prepared from commercial silicon-on-insulator (SOI) wafers, as previously reported [21]. Before transferring a Si NM onto the graphene, the native oxide on the exposed Si substrate was carefully removed by additional wet etching, and the Si surface was then passivated by hydrogen treatment. Then, the Si NM surface was treated with a UV ozone treatment to form a thin surface passivation layer, and the passivated Si NM was stacked onto the graphene contact by means of a dry transfer technique [24]. The top metal electrode was formed by electron-beam lithography and thermal evaporation of Ni/Au (20/30 nm) onto the Si NMs to overlap the bottom graphene electrode. We studied more than a dozen graphene/Si NM heterostructures with a diverse range of thicknesses from 8 to 100 nm, and observed qualitatively similar behavior for each batch of devices.

3. Results and discussion

Figure 1(b) shows an optical image of a fabricated device. The 25 μm strip of monolayer graphene is located inside the dotted lines. The total channel area is defined by the area of overlap between the graphene and the top metal electrode. A cross-sectional transmission electron microscope (TEM) image showing the region from the top drain electrode to the bottom source electrode was taken to investigate the overall integration of the graphene/Si NM/top electrode vertical stack, and to study the interface (figure 1(c)). The well-optimized transfer process including surface pre-treatment produced clean interfaces between graphene and Si, free from native oxide or other contamination layers. In a larger-area TEM image of unoptimized Si NMs transferred onto graphene, contamination was observed, as was native oxide between the graphene and Si (supplementary information). Reducing damage to the silicon substrate during the wet etching of silicon oxide was identified as a key factor in producing atomically clean interfaces.

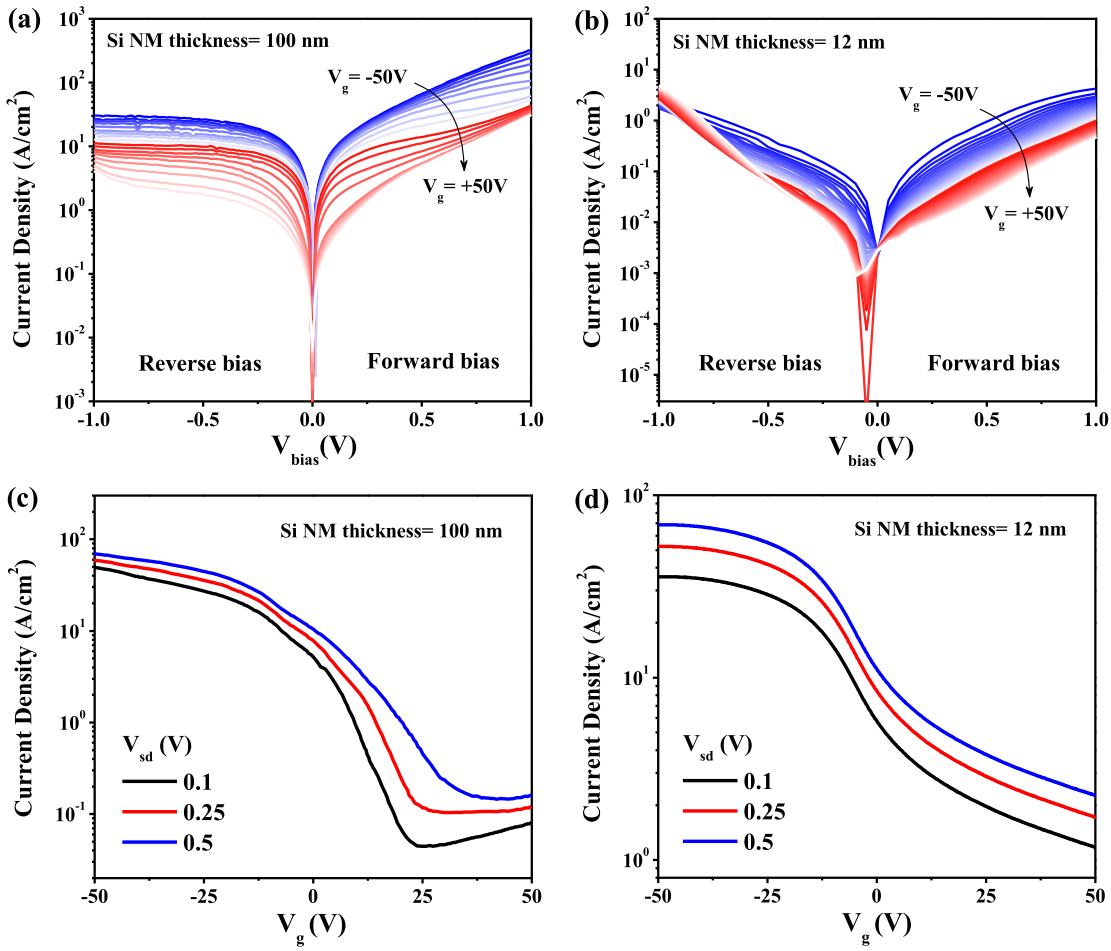

Figure 2. Room-temperature electrical properties of vertical transistors: (a, b) I_{sd}–V_{sd} output characteristics of vertical transistors with Si NM thickness of (a) 100 nm and (b) 12 nm; measured current is normalized by the device area. (c, d) I_{sd}–V_g transfer characteristics of the devices at various biases V_{sd}, for Si NM thicknesses of (c) 100 nm and (d) 12 nm.

The characteristics of current density versus voltage (J–V) were measured at different gate voltages (V_g) in graphene/Si NM/Ni vertical heterostructures, for different thicknesses of Si NMs: 100 and 12 nm (figures 2(a) and (b)). The measured currents were normalized as current densities by dividing them by the area of overlap between the graphene and the top metal electrode. By sweeping the back gate voltage, the output characteristics could be continuously modulated between the off and on states. As back gate potential changed, the current density monotonically decreased with increasing positive gate potential, demonstrating that the electrons were the majority charge carriers because lightly doped Si NMs were used as the tunneling barrier in this vertical transistor. Near the diode turn-on regime, current can be modulated over several orders of magnitude by changing V_g, thereby allowing a switching operation with a large I_{on}/I_{off} ratio. I–V curves for $V_g = -50$ V showed current rectification, although less rectification was observed for thinner devices; this will be further discussed in the context of the results shown in figure 4. In the negative (reverse-bias) regime of source-drain voltage (V_{sd}), the devices displayed conventional FET-like device operation; the current tended to saturate at high reverse bias voltages for thicker Si NM devices. On the other hand, in the forward bias region, the current did not saturate as V_{bias} increased.

Figures 2(c) and (d) show the transfer characteristics (I_{sd}–V_g curves) for both devices studied, and for V_{sd} values of 0.1, 0.25 and 0.5 V. The thicker device exhibited room-temperature on/off current ratios of 10^3–10^4 for all V_{sd} values studied, which is sufficient for typical logic device applications. It is also noteworthy that our graphene/Si NM vertical structure can simultaneously achieve an on/off ratio of 10^4 and a high current density, substantially exceeding the on/off ratios in the range of 2–20 that have been reported for pure graphene transistors [25]. Because the current in the on state is determined by the series resistance of the device rather than the resistance of the graphene/Si NM Schottky barrier, the on-state current density is nearly the same for both devices. In contrast, the off-state current density is significantly reduced for thicker devices owing to the high gate-induced barrier modulation, thereby increasing the on/off ratio for thicker devices. Such thickness dependence seems to be a general behavior of this type of vertical FET

[26, 27]. A higher on/off ratio was obtained for the 100 nm-thick Si NM tunnelling barrier than for the 12 nm-thick barrier. I_{on}/I_{off} is thus determined by the modulation of the electric field across the junctions; more importantly, it can be optimized by varying the barrier- defining parameters, thickness and work function of the metal, because these parameters determine the band profiles for various bias conditions, which influence the device performance.

The band structure at the graphene/Si interface can be schematically illustrated as shown in figures 3(a)–(c), which describe the operation of the device. A gate electric field is applied between the silicon back gate and the grounded top metal electrode. The key factor in device operation is the effective modulation of the graphene/Si NM barrier height and the Fermi level (E_F) near the graphene/Si NM contact, due to the limited density of states of graphene and its weak electrostatic screening effect. When no gate or bias voltage is applied, the Fermi levels of the graphene are located near the bottom of the Si NM valence band (figure 3(a)). The gate voltage V_g between the silicon substrate and the graphene layer changes the carrier concentration in graphene, shifting the Fermi level by $\Delta E_F = \pm h\nu_F\sqrt{|\eta|}$. The sign of the Fermi level shift is determined by the polarity of the gate voltage. Positive V_g elevates the Fermi level of graphene, which causes band bending in the semiconductor and thus leads to an increase in the Schottky barrier (φ_b) at the graphene/Si NM interface (figure 3(b)). In this case, transport is dominated by the Schottky barrier at the graphene/Si NM interface, and thus exhibits high resistance, corresponding to an off state. As a result, a positive gate voltage increases the Schottky barrier height as well as the depletion width, suppressing carrier transport across the vertical stack. In contrast, negative V_g lowers (shifts downward) the Fermi level of the graphene, causing a decrease in φ_b at the graphene/Si NM interface as well as a decrease in the depletion width of the Si NM layer (figure 3(c)). In this case, electrons can pass the Schottky barrier readily by means of thermionic emission or thermionic field emission processes; this enhances charge transport in the vertical device, corresponding to an on state. By varying V_g to switch between the on and off states, the device can be operated as a vertical field-effect tunneling transistor.

To further probe the charge transport through the graphene/Si NM/metal vertical transistor, studies of its temperature dependency were carried out. Current density versus V_g was measured at various temperatures from 300 to 125 K at the fixed V_{sd} of +0.25 V (figures 4(a) and (b)). The current monotonically decreased with decreasing temperature for both cases; however, the J–V_g characteristics of the two samples of different thicknesses (t = 12 and 100 nm) at various temperatures (T) had significant differences. For t = 12 nm (figure 4(b)), the thermal variation of J was found to be within one order of magnitude, and I_{on}/I_{off} remained almost constant throughout the temperature range from 125–300 K; this implies that the dominant contributor to total current was a temperature-independent tunnelling component. In contrast, J_{off} for the thicker Si NM device (t = 100 nm) was dominated by thermal activation above 200 K, and I_{on}/I_{off} varied by two orders of magnitude over the range from 125–300 K. These variable-temperature transport measurements allow the Schottky barrier heights across the graphene/Si NM junction to be determined. According to thermionic emission theory, the diode saturation current is related to the Schottky barrier height by the following equation:

$$I = AA^*T^2 \exp\left(\frac{-q\phi_b}{k_B T}\right)\left[\exp\left(\frac{qV_b}{\eta k_B T}\right) - 1\right], \quad (1)$$

where A is the area of the Schottky junction, A^* is the effective Richardson constant, q is the elementary charge, k_B is the Boltzmann constant, and T is the temperature. ϕ_b can be calculated by investigating the temperature dependence of current in the reverse-bias saturation regime, where[$\exp(qVb/\eta k_B T) \ll 1$]; thus saturation current can be considered independently of bias voltage, and can be simplified as $I_{sat} \propto T^2 \exp(-q\phi_b/k_B T)$ [14]. The saturation current was determined from a logarithmic plot; $\ln(I_{sat}/T^2)$ is plotted against $1000/T$ for different gate bias voltages in figures 4(c) and (d). From equation (1), the Schottky barrier height can be estimated from the slope of these curves as $-\varphi_b/k_B$. The derived Schottky barrier height shows a clear dependence on V_g as well as on tunnelling thickness. At negative V_g, when the device is in an on state, the slopes of the curves are less, indicating the devices' smaller potential barriers. On the other hand, at positive V_g, the slope of the curve is much larger for the t = 100 nm device than for the t = 12 nm device, suggesting a larger φ_b. This change in Schottky barrier height can be largely attributed to modulation of the graphene work function. As the gate bias voltage changes from −50 to +50 V, the derived Schottky barrier height also changes from 270 to 55 meV as the V_g is increased, as shown in inset of figure 5(d). As gate voltage increased from −50 to 50 V, φ_b increased substantially. We attributed the drastic change in φ_b to the electric field effect-induced Fermi level change, ΔE_F. Higher $\Delta\varphi_b$ was obtained for the thicker Si NM, where $\Delta\varphi_b = \varphi_b$(on-state V_g) − φ_b(off-state V_g).

To further investigate the effects of Si NM thickness, we experimentally investigated a large number of GSM devices of varying device sizes and Si NM thicknesses. Off-state ($V_g = -50$ V) and on-state ($V_g = +50$ V) current density data were collected; the on-state current density was nearly constant for all Si NM thicknesses (figure 5(a)). The overall on-state current density typically ranged from 10^1 to 10^2 A cm^{-2}, with a weak dependence on Si NM thickness. We also fabricated graphene/Si NM/graphene Schottky barrier (SB) devices to carry out control experiments; these devices yielded on-state currents about two

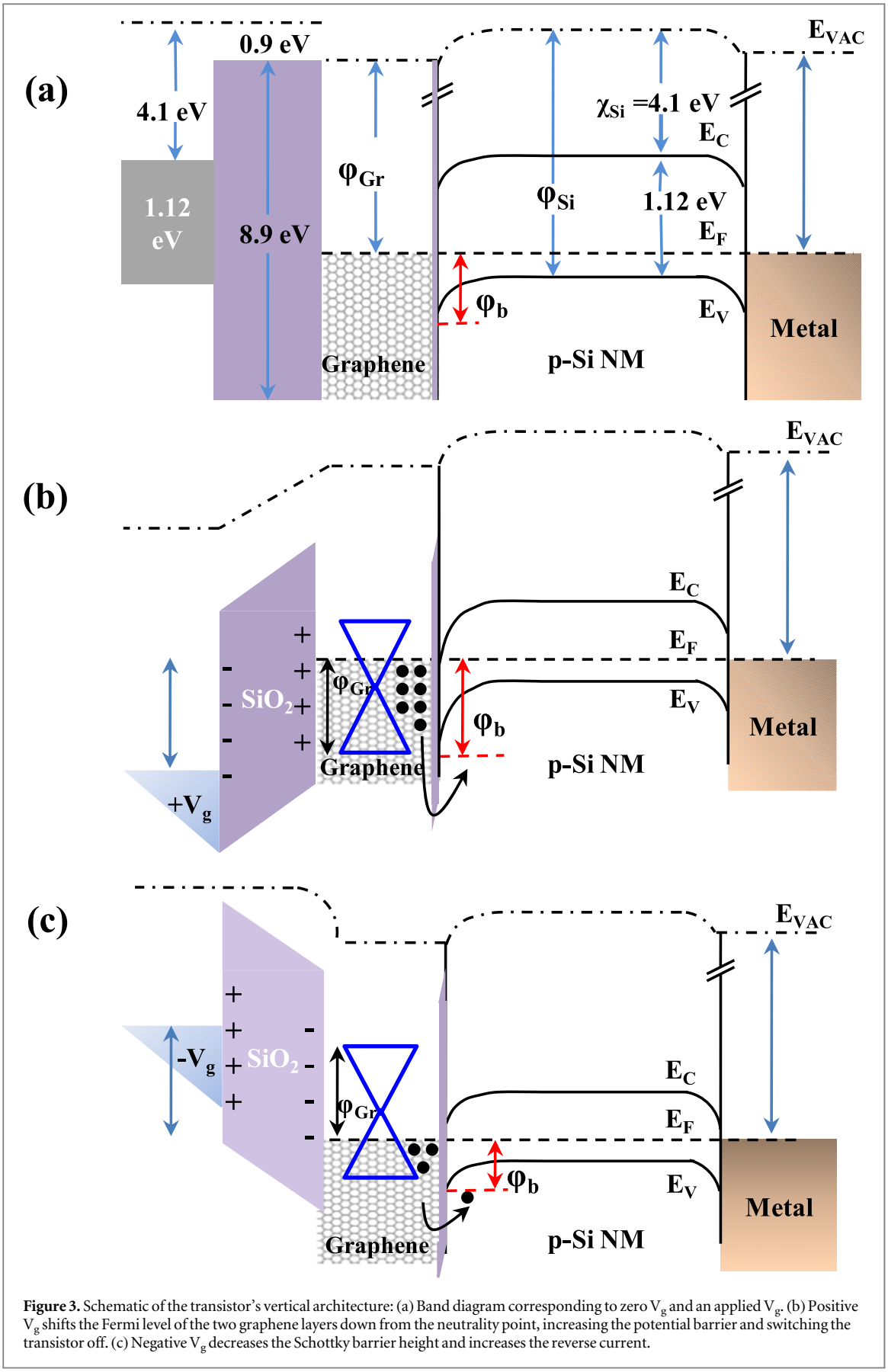

Figure 3. Schematic of the transistor's vertical architecture: (a) Band diagram corresponding to zero V_g and an applied V_g. (b) Positive V_g shifts the Fermi level of the two graphene layers down from the neutrality point, increasing the potential barrier and switching the transistor off. (c) Negative V_g decreases the Schottky barrier height and increases the reverse current.

orders of magnitude smaller than those of the graphene/Si NM/metal Schottky barrier devices, and had lower on/off current ratios. The GSM structure minimized the top Schottky barrier height, thereby reducing its modulation when a low-work-function metal was used. Thus, in this structure, charge transport is dominated by the bottom graphene/Si Schottky barrier height and width, which can be

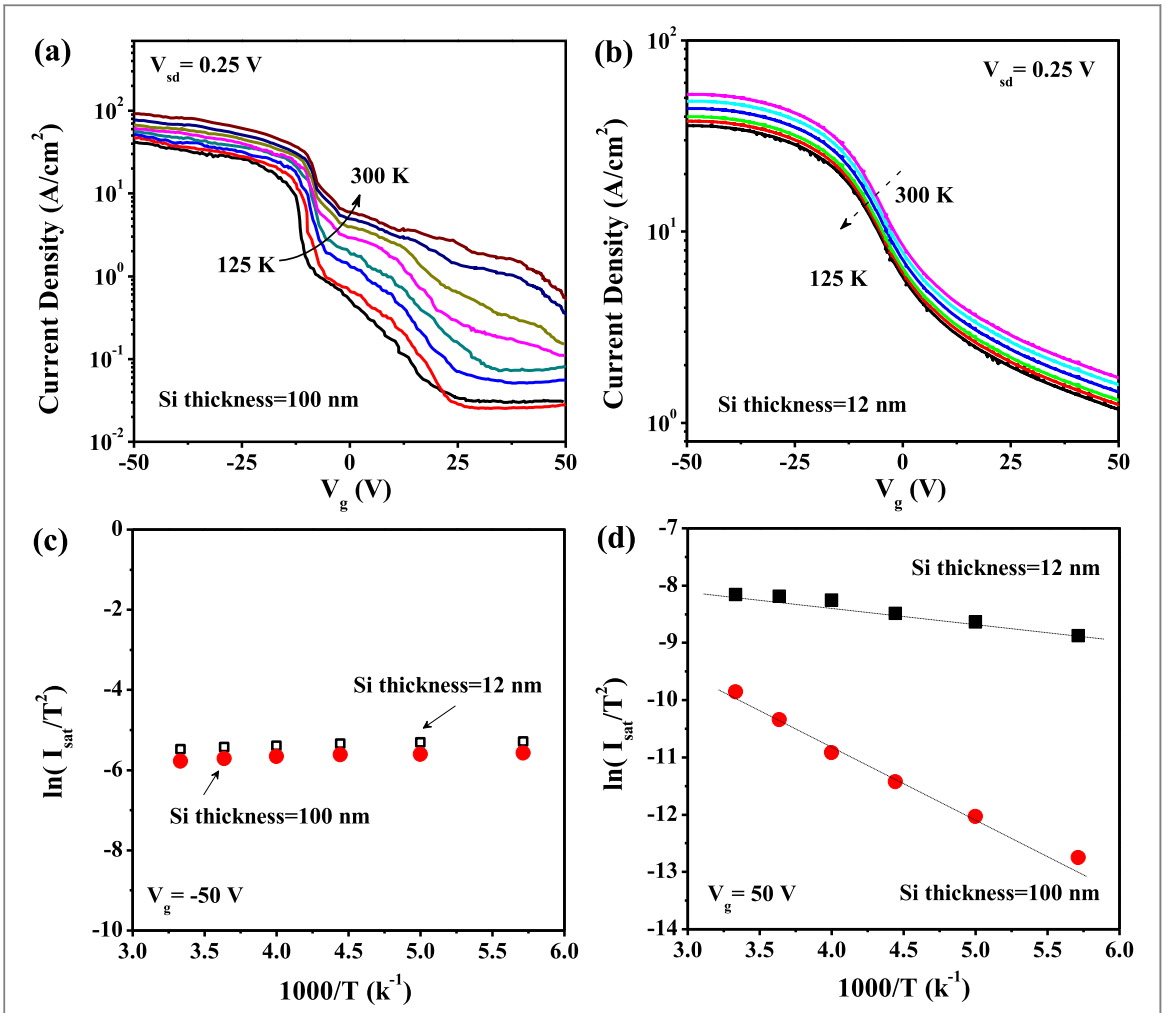

Figure 4. Temperature dependency of the diode's characteristics: (a, b) Semi-log plots of J–V_g characteristics of graphene/Si NM/Ni devices at various temperatures ranging from 125 to 300 K at fixed $V_{sd} = +0.25$ V, for Si NM thicknesses of (a) 100 nm and (b) 12 nm. (c, d) Arrhenius plots of vertical FETs, measured in the (c) on and (d) off states.

effectively modulated by the back gate voltage to yield highly efficient injection and transport. Based on the on- and off-state current density data shown in figure 5(a), on/off current data were plotted; this plot showed that the room-temperature on/off current ratios of the VFETs strongly depended on the Si NM thickness. The temperature dependence of the conductance was studied for graphene/Si NM/metal devices of different Si NM thicknesses ranging from 8 to 100 nm. A series of measurements were carried out to determine the amplitude of the barrier height modulation, $\Delta\varphi_b$, versus changes in the thickness of the Si NM (figure 5(c)). The thickness dependence of the Schottky barrier height $\Delta\varphi_b$ determined from Arrhenius plot and on-off ratio exhibits good coincidence with figure 5(b). Figures 5(b) and (c) further confirm that the modulation of the Schottky barrier height at the graphene/Si NM interface plays a dominant role in the switching operation of the vertical transistor. In general, it was found that the room-temperature on/off ratio of the vertical transistors exceeded three orders of magnitude for a relatively thick Si NM (>70 nm), and gradually decreased to 10 when the Si NM thickness was reduced below 10 nm. Reduced on/off ratios in thinner NMs have been reported previously, and have been attributed to metal-induced lowering of the Schottky barrier height [12]. This lowering, which is also referred to as the Schottky effect, can contribute to the image force lowering and quantum capacitance of graphene. Both image force and quantum capacitance are inversely proportional to channel length, which in this case corresponds to the thickness of the Si NM [28, 29]. With decreasing Si NM thickness, the entire channel becomes increasingly dominated by this effect, thereby reducing $\Delta\varphi_b$ and resulting in a smaller on/off ratio. The room temperature on/off ratio of $>10^3$ achieved in our devices was about two orders of magnitude smaller than the on/off ratio achieved in recently reported barristors [14]. This might be attributed to the presence of interface defects at the graphene/Si NM interface in our devices; if so, this could be improved by the use of cleaner interfaces in future studies. Ideality factors were determined for all values of Si NM layer thickness (figure 5(d)). Deviation from ideal diode behavior may be attributed to graphene/Si NM interface defects,

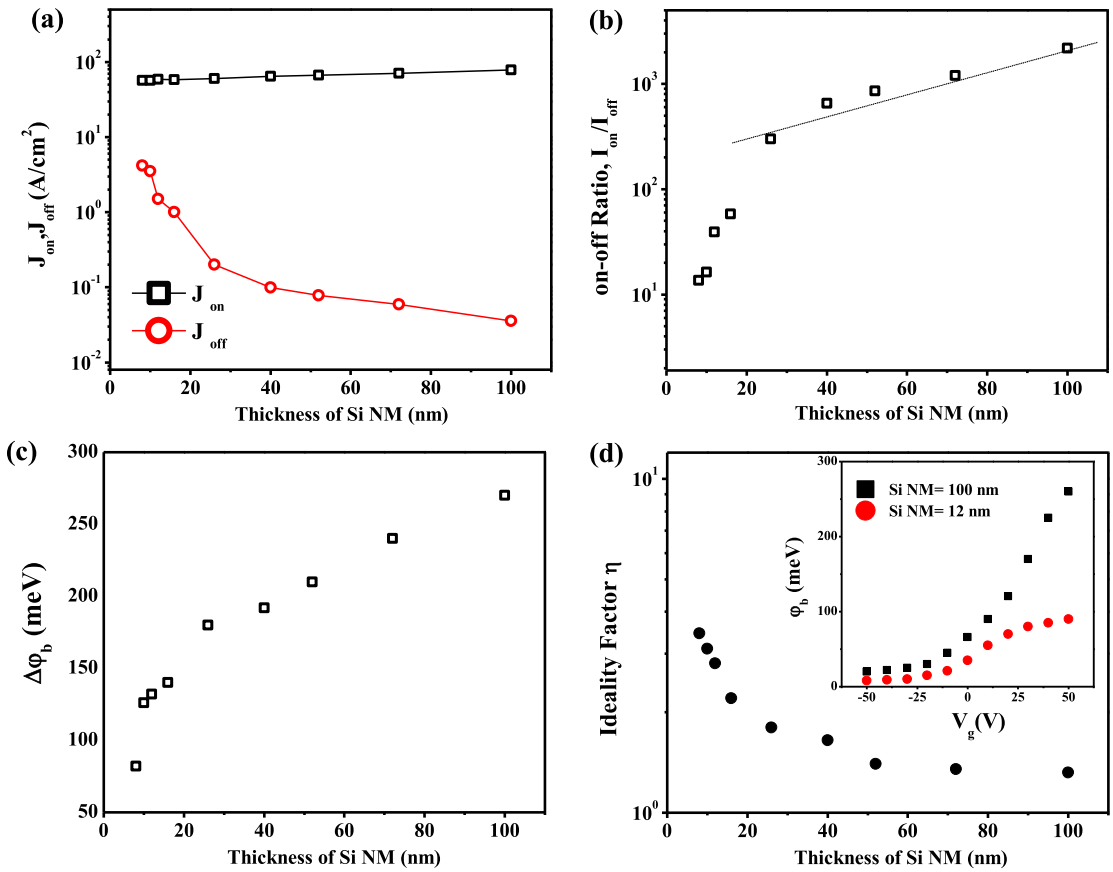

Figure 5. Effects of Si NM tunneling layer thickness on the vertical transistor: (a, b) on/off current and on/off current ratio versus Si NM thickness. (c) Amplitude of barrier height modulation $\Delta\varphi_b$ versus Si NM thickness. (d) Ideality factor η versus Si NM thickness, (d, inset) Schottky barrier heights under V_g modulation.

and also probably to the electrostatic screening effect of the top Si NM/metal contact due to the ultrathin Si channel thickness (length). The ideality factor was close to unity for devices with Si NM thickness above 26 nm, corresponding to near-ideal Schottky diode behavior.

4. Conclusions

We have demonstrated integration of a vertical tunneling transistor by implementing ultrathin Si nanomembranes in GSM heterostructures; this can enable a new design for graphene-based vertical transistors. The transport properties of the graphene/Si NM/metal vertical heterostructures were investigated over a wide range of Si NM thicknesses from 8 to 100 nm. The devices showed a maximum on/off current ratio (I_{on}/I_{off}) of up to $\sim 10^3$ with a current density of 10^2 A cm^{-2} at room temperature for relatively thick Si NM (>70 nm), thereby satisfying the requirements of high-performance logic applications. The change in the Schottky barrier height was higher for thicker Si NMs (270 meV for a 100 nm Si NM, compared to 87 meV for a 12 nm Si NM), and it was found that the modulation of Schottky barrier height, $\Delta\varphi_b$, is a key factor to achieve larger current modulation of the device. By using the device scheme developed herein, a variety of materials can be explored and implemented in the future to enhance device performance.

Acknowledgments

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Appendix. materials and methods

The monolayer graphene was grown by CVD on copper foil at 1035 °C and transferred onto a Si/SiO_2 substrate. Next, the graphene layer was patterned into strips 25 μm wide and 100 μm long by optical photolithography and oxygen plasma etching to outline drain electrodes. The silicon substrate also served as a global back gate. In a parallel process, free-standing and isolated Si NMs were prepared from commercial SOI wafer, that is, Si (100 nm)/SiO_2 (300 nm)/Si

(wafer) using polydimythylsiloxane (PDMS) stamping. Details of the transfer process have been described elsewhere [21]. Different batches of Si NMs were prepared by two-stage oxidation (thermal and UV) varying the thickness of Si NMs in a range from 100-8 nm and transferred onto a bare Si chip coated with $\sim$1 μm of polypropylene carbonate (PPC) (Sigma-Aldrich, CAS 25511-85-7). The transferred Si NMs were examined by optical microscopy and atomic force microscopy (AFM) (Supplementary Information S2). Before transfer onto graphene, native oxide on the exposed Si substrate was carefully removed by additional wet etching followed by the passivation of the Si surface with hydrogen treatment in a controlled atmosphere. Silicon can easily be oxidized by native oxygen, contaminating the interface. Before transfer, the Si NM surface was passivated by ozone in a UV ozone chamber. The presence of a thin $\sim$1 nm passivation layer was confirmed by TEM; this layer is believed to serve as a surface protection layer. The PPC was then manually peeled from the Si substrate and placed on a transparent elastomer stamp. After that, the Si NMs were transferred onto pre-patterned graphene stripes by a dry transfer technique. The device was annealed in forming gas (5% H_2, 95% Ar) for 1 h at 200 °C in order to improve the interface properties. By using electron-beam lithography and thermal evaporation, a Ni/Au (20/30 nm) metal electrode was fabricated on top of the Si NMs to overlap with the bottom graphene.

The cross-sectional TEM sample was prepared using focused ion beam milling and characterized by a JEM-200F TEM operating at 300 kV. Tapping-mode AFM measurement was done by an XE-100 (Park Systems). The I-V characteristics of the graphene-based VFETs were measured by a Keithley 4200 SCS parameter analyzer as a function of gate voltage at both room temperature and low temperature (300-125 K) in a N_2 atmosphere under high vacuum.

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