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Photo-patternable ion gel-gated graphene transistors and inverters on plastic

Seoung-Ki Lee[1,2], S M Humayun Kabir[3], Bhupendra K Sharma[2], Beom Joon Kim[3], Jeong Ho Cho[3,4] and Jong-Hyun Ahn[2]

[1] School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 440-746, Korea
[2] School of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea
[3] SKKU Advanced Institute of Nanotechnology (SAINT), Sungkyunkwan University, Suwon 440-746, Korea
[4] School of Chemical Engineering, Sungkyunkwan University, Suwon 440-746, Korea

E-mail: jhcho94@skku.edu and ahnj@yonsei.ac.kr

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Abstract

We demonstrate photo-patternable ion gel-gated graphene transistors and inverters on plastic substrates. The photo-patternable ion gel can be used as a negative photoresist for the patterning of underlying graphene as well as gate dielectrics. As a result, an extra graphene-patterning step is not required, which simplifies the device fabrication and avoids a side effect arising from the photoresist residue. The high capacitance of ion gel gate dielectrics yielded a low voltage operation (~2 V) of the graphene transistor and inverter. The graphene transistors on plastic showed an on/off-current ratio of ~11.5, along with hole and electron mobilities of 852 ± 124 and 452 ± 98 $cm^2\ V^{-1}\ s^{-1}$, respectively. In addition, the flexible graphene inverter was successfully fabricated on plastic through the potential superposition effect from the drain bias. These devices show excellent mechanical flexibility and fatigue stability.

S Online supplementary data available from stacks.iop.org/Nano/25/014002/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

Graphene has attracted considerable attention due to its optical transparency, mechanical flexibility, and high carrier mobility [1–5]. To utilize such properties of graphene in large-area flexible electronic applications, it is important to develop clean and simple device fabrication procedures that do not leave residues on graphene, because the resulting device is seriously affected by photoresist residue during the photolithography process, and that allow the printing of device components at low temperature [6–9]. However, this is still significantly challenging.

The formation of gate dielectric layers also remains an obstacle to flexible devices. For example, conventional gate oxide films need a high-temperature process, which cannot be applied to a heat-vulnerable plastic substrate, and are difficult to form uniformly on the top of graphene without a special buffer layer due to the uneven surface energy of graphene [10, 11]. As an alternative, we recently described the preparation of graphene transistor arrays on plastic substrates using an ion gel gate dielectric [12], which is a physical gel composed of ionic liquids in a polymer matrix. Although these devices exhibited high carrier mobility at low operating voltages, their performances were vulnerable to temperature changes and substrate bending. These sensitivities arose because the ion gel employed in that report was formed simply by the physical association of a block copolymer film. The development of a solution process for preparing gate dielectric layers that provide for excellent and stable device performance is critical in achieving practical applications of graphene in the electronics industry.

To address this issue, we demonstrated self-aligned flexible graphene transistors and inverters based on photo-curable ion gel gate dielectrics. The photo-patternability of an

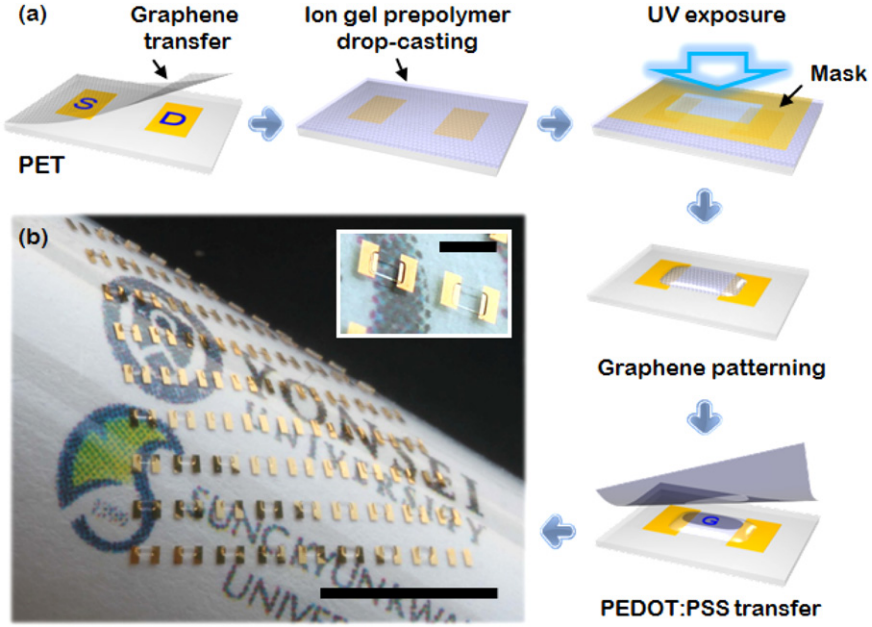

Figure 1. (a) Schematic diagram of the fabrication procedure for flexible graphene transistors with photo-patternable ion gel gate dielectrics on a PET substrate. (b) Large-area flexible graphene transistor array (scale bar: 5 mm). The inset shows the optical image of a completed device unit (scale bar: 1 mm).

ion gel can simplify the fabrication process by eliminating the extra graphene-patterning step, because it is used as a negative photoresist to pattern the graphene. The self-aligned graphene transistors exhibited low-voltage operation with a high on-current due to the high-capacitance electric double layer formed at the ion gel/graphene interface [13]. In addition, flexible graphene inverters were successfully fabricated on plastic and showed excellent mechanical flexibility and fatigue stability.

2. Experimental details

The fabrication steps for top-gate graphene transistors with photo-patternable ion gel gate dielectrics on a plastic substrate are shown in figure 1(a). High-quality monolayer graphene was synthesized over a large area of Cu foil, as described previously [12, 14]. A poly(methylmethacrylate) supporting layer was spin-coated onto this graphene monolayer, and the Cu foil was chemically etched using an aqueous 0.1 M ammonium persulfate solution. The monolayer graphene was then transfer printed onto a polyethylene terephthalate (PET) substrate containing the source and drain electrodes (5 nm Cr/50 nm Au) formed by thermal evaporation. Due to the van der Waals force between graphene and the PET substrate, monolayer graphene can be formed successfully on the substrate. To avoid cracking and damage to the graphene, a 'second PMMA coating' step was carried out before removing the polymer supporting layer [15]. The quality of the transferred graphene was verified by Raman spectroscopy (supplementary information, figure S1 available at stacks.iop.org/Nano/25/014002/mmedia). Onto the graphene film with a Au source and drain contact, a UV-crosslinkable ion gel ink comprising the poly(ethyleneglycol) diacrylate (PEG-DA) monomer, the 2-hydroxy-2-methylpropiophenone (HOMPP) initiator, and the 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM:TFSI) ionic liquid (weight ratio of 8:4:88) was drop-cast [16]. A square-patterned photomask was then placed over the ion gel layer, and the ion gel was exposed to UV light (100 mW cm^{-2} at 365 nm) for 5 s. Upon UV exposure, HOMPP generates radicals that can react with the acrylates in PEG-DA monomers to initiate polymerization. As a result, a chemically cross-linked ion gel was photo-patterned only in the areas exposed to UV light, whereas the ion gel ink under the unexposed region was washed away with chloroform. Then, the graphene portion uncovered by ion gel was removed by oxygen plasma for 2 s. During the plasma etching process, the photo-patternable ion gel acted as a negative photoresist for the graphene pattern. The channel width was controlled using photomasks with various pattern sizes. Following this method, almost all devices were successfully patterned with a minimum resolution of $\sim$30 μm. Finer patterns would be possible using more elaborate facilities. To form a gate electrode, poly(3,4-ethylenedioxythiophene) oxidized with poly(4-styrenesulfonate) was transferred to the top of the photo-patterned ion gel layer using polydimethylsiloxane. Figure 1(b) shows a photograph of a UV-patterned top gate graphene transistor array on a PET substrate.

3. Results and discussion

Figure 2(a) shows the typical drain current (I_D)-drain voltage (V_D) characteristics at five different gate voltages (V_G) of a graphene transistor fabricated on a PET substrate in the

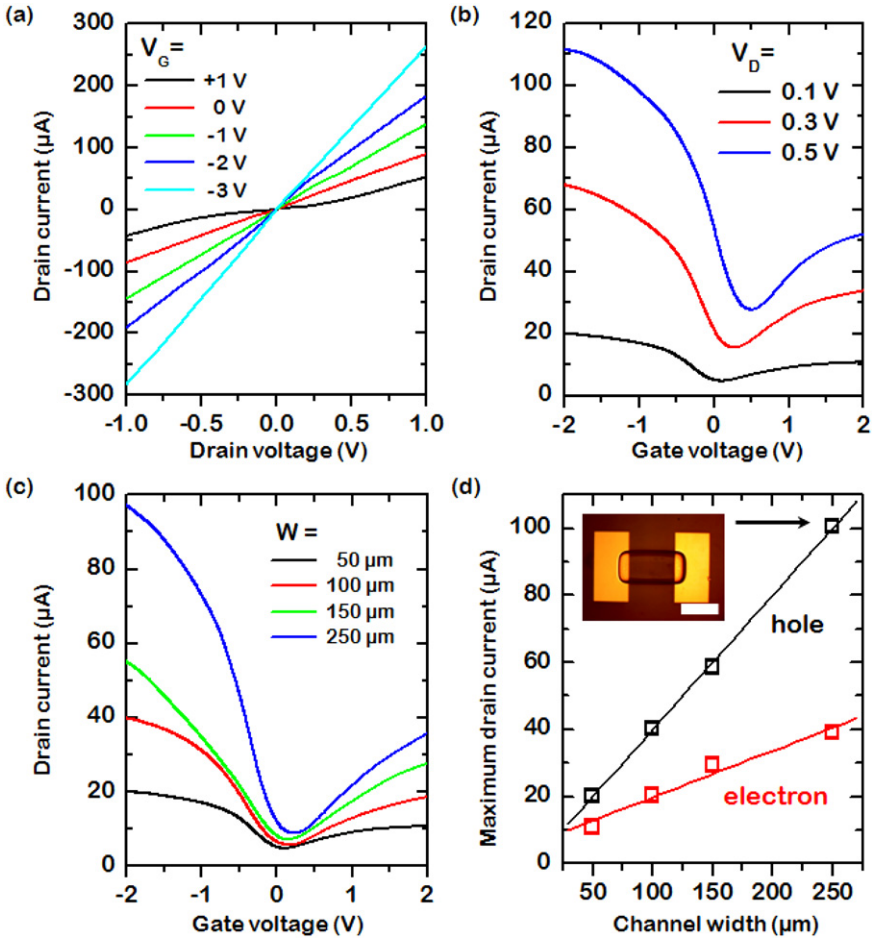

Figure 2. (a) Output characteristics of graphene transistors with photo-patternable ion gel gate dielectrics at five different gate voltages ranging from +1 to −3 V. (b) Transfer characteristics of the devices at three different values of V_D (0.1, 0.3, and 0.5 V). (c) Transfer characteristics of the devices with four different channel widths of 50, 100, 150, and 250 μm. (d) Maximum hole and electron currents as a function of the channel width of the devices. The inset shows a top view of a self-aligned graphene transistor (scale bar: 300 μm).

top-gate configuration. The device exhibited a linear increase in drain current induced by the gate voltage, indicating the lack of significant Schottky barriers between the drain electrode and the graphene channel [17]. The small Schottky barrier for the electron and hole is a typical contact for metal/zero band gap semiconductor junctions [18]. A large drain current above 250 μA was obtained at a low V_D of 1 V and V_G of −3 V, which is attributed to the very large capacitance of the ion gel gate dielectrics (7.29 μF cm^{-2} at 10 Hz). This huge capacitance induced more than 10^{13} charges per square centimetre under the application of a few volts, which allows low-voltage operation of the graphene transistors. Figure 2(b) shows I_D as a function of V_G at three different values of V_D for the graphene transistors. The device operated at low voltages below 3 V with a high on-current. V-shaped ambipolar behaviour was observed in the gate dependence of I_D, where positive and negative V_G regions represented the electron and hole transport, respectively. This ambipolar behaviour is directly related to the characteristic electronic structure of graphene: due to the zero band gap of graphene, the Fermi level can be continuously driven between the conduction band (electron transport) and valence band (hole transport) of cone-shaped band structure by tuning the gate bias. Under an applied negative gate bias, the Fermi level was down-shifted below the Dirac point and hole carriers were generated. In contrast, the Fermi level was up-shifted at positive gate bias and electron carriers were generated [19, 20]. Thus, the hole and electron carriers were completely dependent on the applied gate bias. The Dirac voltage (V_{Dirac}), where the electron and hole make equal contributions to the transport, was found to be almost zero at a drain voltage of 0.1 V. The value of V_{Dirac} shifted towards the positive voltage direction with increasing drain voltage (figure 2(b)). This is because a positive increase in V_D at a given V_G can facilitate hole injection from the drain electrode for an ambipolar material (in general, hole injection takes place when $V_G - V_D$ becomes more negative than the hole injection threshold voltage) [21]. The ambipolarity in GFETs having controllable Dirac voltages with the applied drain bias is a great advantage in fabricating logic circuits. Using this voltage-driven Dirac voltage-shifting mechanism, we fabricated an inverter on a flexible substrate.

Under an applied electric field in the top-gate electrode, electric double layers (EDLs) were formed at both the

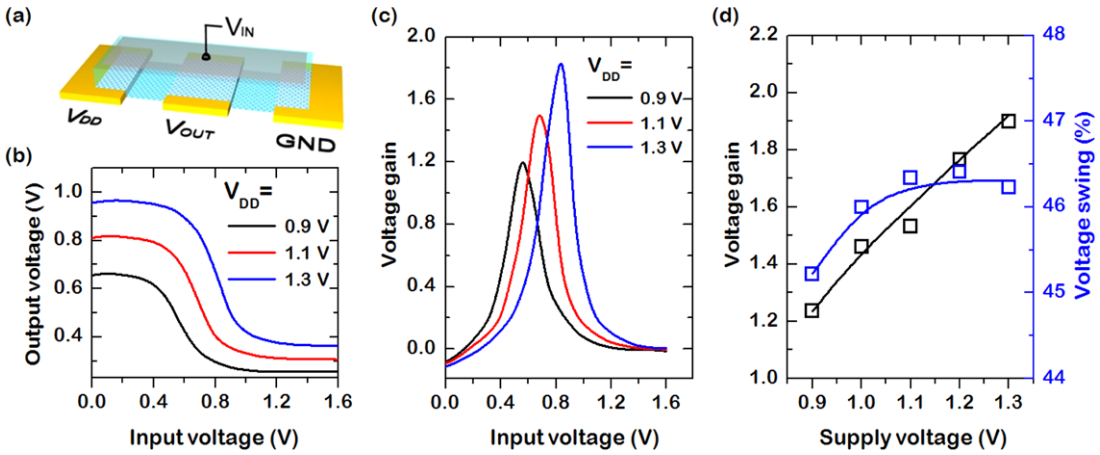

Figure 3. (a) Schematic diagram of a complementary inverter based on two graphene transistors with photo-patternable ion gel gate dielectrics. (b) Voltage transfer characteristics and (c) corresponding voltage gain of a complementary graphene inverter at three different values of V_{DD} (0.9, 1.1, and 1.3 V). (d) Voltage gain and swing of a complementary graphene inverter as a function of V_{DD}.

gate/ion gel and ion gel/graphene interfaces. For example, the application of a negative voltage to the gate electrode induced positive (EMIM) ions at the gate/ion gel interface, whereas negative (TFSI) ions were driven to the graphene channel, and vice versa. The important feature of the ion gel-gated transistor is the formation of these two EDLs in series, which are located at the gate/ion gel and ion gel/active layer interfaces with a charge-neutral diffuse layer between them. Since the capacitance of this diffuse layer is negligible, the interfacial capacitance of the ion gel can then be modelled as a serial combination of an electric double layer capacitance (C_{EDL}) and a quantum capacitance of the graphene (C_q) [22]. Therefore, the potential drop across the two capacitors is given by

$$|V_G - V_{G,min}| = \frac{h v_F \sqrt{\pi n}}{e} + \frac{ne}{C_{EDL}}$$

where h is the reduced Planck's constant, v_F is the Fermi velocity (1.1×10^6 m s^{-1}), e is the electron charge, and n is the charge density. From the plots of conductivity (σ) versus n, the carrier mobility was calculated according to $\mu = (d\sigma/dn)/e$. Although the performance of GFETs is limited by carrier scattering effect from the rough surface profile of a plastic substrate [23], the device shows an on/off-current ratio of ~11.5 and high hole and electron mobilities of 852 ± 124 and 452 ± 98 cm^2 V^{-1} s^{-1}, respectively. Note that higher carrier mobilities of graphene transistors using photo-patternable ion gel gate dielectric were achieved than previous electrolyte-gated GFETs results [12, 24–26]. Interestingly, the result is comparable to those devices using the ion gel gate dielectric based on a triblock copolymer, despite using the same batch of graphene. This is probably because the UV-patterning of an ion gel avoids the residue of both solvent and photoresist at the graphene/ion gel interface which can act as charge trap sites, resulting in a decreased transistor performance.

One of the major advantages of a photo-patternable ion gel is that it can be used as a negative photoresist for the patterning of graphene as well as the gate dielectrics. This eliminates the additional fabrication step for the underlying graphene pattern. Figure 2(c) shows the transfer characteristics of the graphene transistor with different channel widths. For a channel width of 50 μm, maximum hole and electron currents were measured to be 20 and 10.7 μA, which increased to 97.3 and 35.7 μA, respectively, for the 250 μm channel width. When the channel width was increased at a fixed channel length, the maximum electron and hole currents increased, as summarized in figure 2(d). However, the field effect mobility showed an inverse dependence on channel width. Namely, the larger channel width yields lower carrier mobility, which may be due to the edge scattering and electrostatically induced charge accumulation [27]. These relationships between the channel dimension and electrical property indicate that the device characteristic can be modulated by electronic gate coupling over the channel area.

The complementary inverter was demonstrated by connecting two photo-patternable ion gel-gated graphene transistors, where one of the transistors was connected to the supply voltage (V_{DD}) and the other contacted to the ground (figure 3(a)). When the identical ambipolar transistors were connected in series, there was a significant voltage drop across the transistor connected to V_{DD}. Thus, another transistor connected to ground operated at a lower V_{DD}. Through this potential superposition effect from the drain bias, the V_{Dirac} of graphene transistors connected in series can be split [21, 28, 29]. Therefore, the two transistors operate in the complementary mode between Dirac voltages. Figures 3(b) and S2 (supplementary information available at stacks.iop.org/Nano/25/014002/mmedia) show the voltage transfer characteristics of the graphene inverter for both positive and negative drain voltages on the PET substrate, indicating good inverter action, in which the output voltage (V_{OUT}) was switched inversely as the input voltage (V_{IN}) was swept. The output voltage is given by the relationship $V_{OUT} = V_{DD}/(1 + R_1/R_2)$. In the region between two Dirac voltages, the increase in the V_{IN} increases R_1 but decreases R_2, resulting in a strong increase in the ratio R_1/R_2. As a consequence,

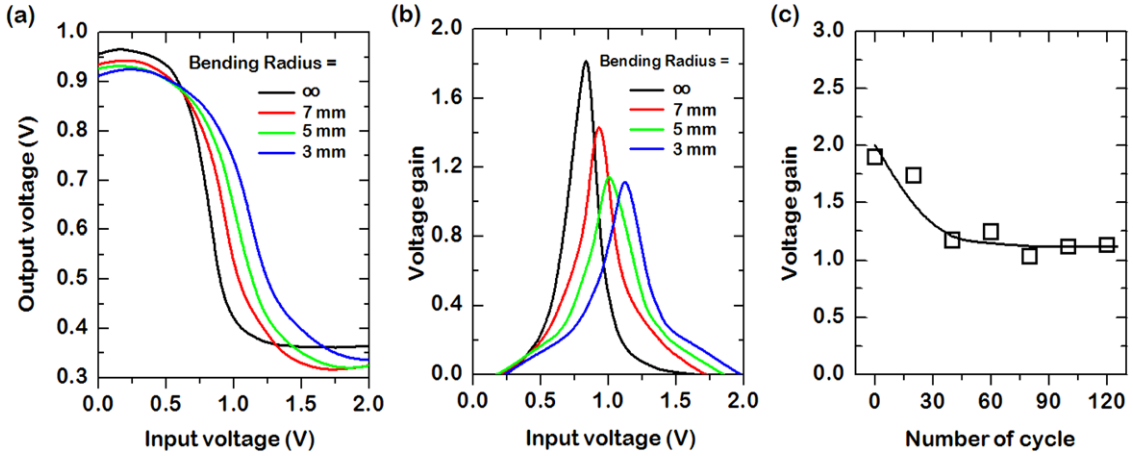

Figure 4. (a) Voltage transfer characteristics and (b) corresponding voltage gain of a complementary graphene inverter as a function of bending radius (7, 5, and 3 mm). (c) Voltage gain as a function of cycle (bending radius = 5 mm).

V_{OUT} decreases with increasing V_{IN}, which gives rise to the voltage inversion. The corresponding voltage gain, which is defined by $-dV_{OUT}/dV_{IN}$, of the graphene inverter is shown in figure 3(c) and the gain distribution histogram from the inverter array (∼total 49 ones) is depicted in supplementary information, figure S3 (available at stacks.iop.org/Nano/25/014002/mmedia). The inverter gain increased linearly with V_{DD} from 0.9 to 1.3 V (figure 3(d)). In particular, the inverter showed a voltage gain of 1.90 at $V_{DD} = 1.3$ V, which is sufficient to drive the next stage component in a logic circuit. Moreover, the voltage swing, which is defined as $[V_{OUT,max} - V_{OUT,min}]/V_{DD} \times 100\%$, increased slightly from 45% to 46% when increasing V_{DD} from 0.9 to 1.3 V (figure 3(d)). The improvement in voltage swing and gain can be attributed to a high capacitive efficiency, which increases with supply voltage (V_{DD}). Further increments of V_{DD} caused a degradation of the voltage swing as it introduced minority carrier injection in the channel, which causes an increased off-state current [29]. Unfortunately, we were not able to achieve a reasonable noise margin value because signal inversion occurs far over half of the V_{DD} and this device structure contains large parasitic capacitances due to an unexpected overlap between the gate and the source (or drain) electrodes. Further optimization of the device configuration would improve this drawback.

The mechanical flexibility of the graphene inverters on a PET substrate was investigated by bending the substrate into a radius as small as 3 mm. The graphene inverter was bent along directions parallel and vertical to the TFT channel length. A custom-built bending apparatus was used to carry out the bending, and electrical measurements were taken while the device was in the bent state. Figure 4(a) shows the voltage transfer characteristics of the flexible graphene inverter at bending radii of 7, 5, and 3 mm when bent in the parallel direction. The voltage transfer characteristics in the initial flat and bent states suggest that the voltage inversion gets worse with bending radius, which may be caused by damage in the graphene channel and/or micro-cracks in the Au electrodes. In the case of the vertical direction, however, the inverter exhibits better mechanical stability even under the same bending radii, as shown in supplementary information, figure S4 (available at stacks.iop.org/Nano/25/014002/mmedia). This anisotropic bendability is due to the fact that the effective strain on the device depends on the orientation of bending. Even for a bending radius of 3 mm, however, the graphene inverter exhibited a voltage gain greater than unity due to the excellent flexibility of the graphene and ion gel. The corresponding gains for the initial flat and bent states are exhibited in figure 4(b). Finally, the fatigue stability of the inverters was tested (figure 4(c)). The inverter gain decreased from 1.9 to 1.1 after 40 cycles but then showed negligible changes up to 120 cycles. Overall, the bending and fatigue tests demonstrated the stable and reliable operation of the flexible graphene inverters. There are a few reports on graphene transistors and logic gates [30–32], in all of which the circuits either required large operating voltages, had to be operated under vacuum conditions, or required high-temperature metal deposition with a complex fabrication procedure.

4. Conclusion

In this work, we introduced a photo-patternable ion gel-gated graphene transistor and inverters on a plastic substrate. For a particular $V_{DD} = 1.3$ V, the voltage gain and swing reached 1.9 and 46%, respectively, which indicates good inverter switching characteristics at a low operating voltage. This work signifies a relatively simple fabrication technique for logic components, because it does not require a vacuum, high-temperature manufacturing process, and avoids photoresist residue in defining the channel regions. Most importantly, we were able to fabricate a large-area device with uniform performance using chemical vapour deposition-grown graphene.

Acknowledgments

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