



# Graphene based field effect transistors: Efforts made towards flexible electronics



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## ARTICLE INFO

### Article history:

Received 19 February 2013

Received in revised form 15 July 2013

Accepted 17 August 2013

The review of this paper was arranged by editor Prof. S. Cristoloveanu

### Keywords:

Graphene

Field effect transistor

Flexible electronics

Chemical vapor deposition

## ABSTRACT

The integration of flexibility in existing electronics has been realized as a key point for practical application of unusual format electronics that can extend the application limit of biomedical equipments and of course daily routine kind of electronic devices. Graphene showed the great potentiality for flexible format owing to its excellent electronic, mechanical and optical properties. Field effect transistor (FET) is a basic unit for digital and analog electronics thus enormous efforts have been attempted to fabricate the flexible FETs in order to get the high performance. This article reviews the recent development of graphene based FETs including the fabrication and active layers material compatibility in flexible format.

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## 1. Introduction

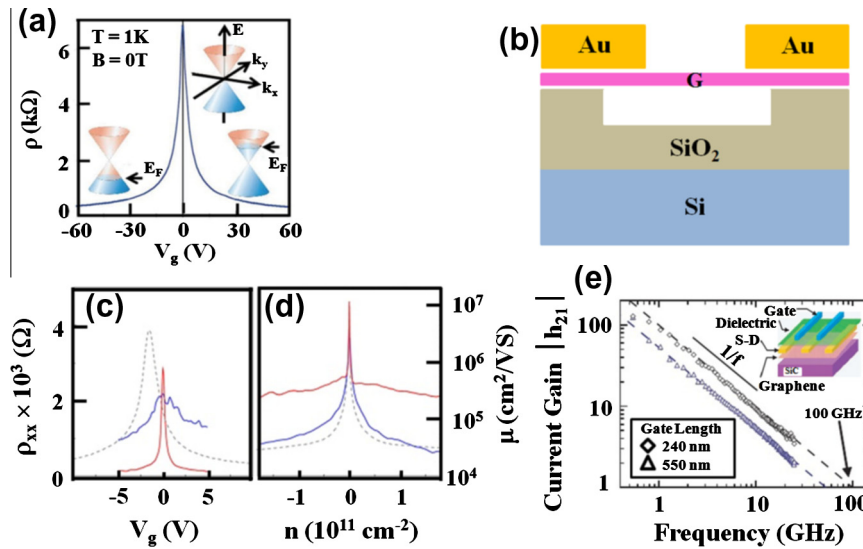
Bendable electronic circuitry that can be fabricated on a large area has received much interest as it enables special applications which are difficult to realize with conventional wafer based Si technology due to its poor mechanical endurance, large area non-uniformity and high temperature processing [1–6]. In this regard, new materials compatible with high strain values and architecture designs that would allow these materials to be integrated in hybrid system devices are needed for next generation electronics [7–18]. Normally, in the fabrication of such electronic devices, it would be desirable to use a multifunctional material which can show semiconducting properties, high conductivity comparable to those of conventional metals, and high strain endurance to meet the requirement of flexible electronics [19,20]. The metallic conductivity of the material would allow replacement of the conventional metals used for contact electrodes, while its excellent semiconducting properties would provide an active region.

In the semiconductor industry, the transistor is recognized as the most important basic building block of all electronic circuitry in digital and analogous electronics such as microprocessors, DRAMs and flash memories, active matrix displays, mobile communications and other signal processing and logic functions. Normally, transistor performance is evaluated in terms of field effect

mobility ( $\mu$ ), on current ( $I_{on}$ ), off current ( $I_{off}$ ), on/off ratio ( $I_{on}/I_{off}$ ), threshold voltage ( $V_t$ ), and subthreshold swing (SS) [21–23]. Some of these parameters may become more important than the others depending on the desired application, and this priority in importance further helps in material selection and fabrication process. In few applications, particularly in active matrix displays, a high  $I_{on}/I_{off}$  is required whereas a high drive current is only needed if switching speed is critical [24,25]. Existing electronics has evolved on the Si technology due to its compactness, stability and efficient performance of devices. Most conventional integrated circuits (ICs) are based on single-crystal silicon, while active matrix display applications are based on amorphous silicon (a-Si). Si technology has continued to advance with the miniaturization of electronic devices [26]. However, this advancement has been limited by various scientific and technical issues [27]. According to Moore's law in each new generation, the device size should reduce by 3%, the chip size should increase by 50% and every three years number of components on a chip should increase by 4 times. The most important feature of Si which makes it the first choice for semiconductor industry is its native oxide ( $\text{SiO}_2$ ). For the future miniaturization of Si devices and to fulfill the Moore's law the device size should reduce more and more which demands the decrement of gate oxide thickness up to few layers of Si atom and then eventually to zero. It is not practically possible to get the zero or 1–2 atomic thick gate oxide thus there is a limit for scaling down the Si based devices [27]. Further, the realization of flexible devices based on existing Si technology has become

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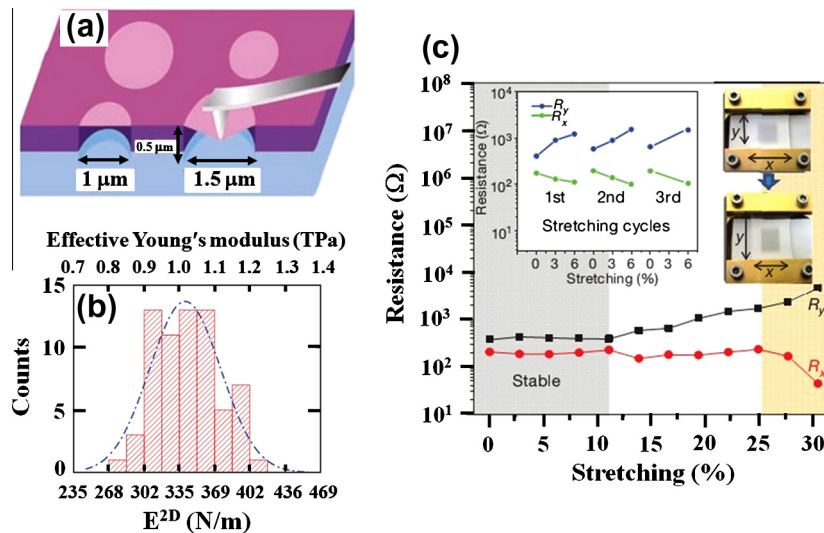
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**Fig. 1.** (a) Continuous variation of carrier concentration for monolayer graphene by the application of negative and positive biases indicating the tuning of carriers from one type to another [35]. (b) Schematic cross-sectional image of as fabricated suspended graphene device on  $\text{SiO}_2/\text{Si}$  substrate showing the partially etched  $\text{SiO}_2$  below the graphene [50]. (c) Variation of resistivity as a function of applied gate voltage before (blue) and after current annealing (red) [50]. Gray dotted line shows the high mobility device data on the substrate. (d) Variation in calculated mobility of suspended graphene device as a function of carrier density before (blue) and after (red) annealing [50]. Gray dotted line shows the mobility variation for unsuspended graphene. (e) Variation of ratio of small-signal drain and gate currents  $|h_{21}|$  (short circuit current gain) with frequency and inset shows the schematic cross-sectional image of the top gated graphene FET exhibiting  $n$ -type characteristics [51]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

difficult due to its rigid and compact fabrication. The graphene-based technology may make an alternative to overcoming such limitations of Si technology. Graphene, a one-atom-thick planar sheet in a two-dimensional (2D) network of  $\text{SP}^2$  hybridized carbon atoms packed into a hexagonal structure, has recently attracted much attention in the scientific community for its potential applications in printed flexible electronics due to its excellent electronic and mechanical properties [28–35]. Fabrication of field effect transistors (FETs) using graphene as an active component can significantly contribute in the evolution of next generation flexible electronics [36–38]. In addition to transistors, graphene can be used as transparent electrodes in solar cells, organic light emitting devices and other electronic devices [39–43]. Graphene was first demonstrated in 2004 by Novoselov et al. [31] using an

unconventional method which involved the physical peeling of layers from bulk graphite using scotch tape and transferring the graphene layers on a  $\text{SiO}_2$  substrate. Although this method was sufficient for preliminary investigation of graphene properties, but it was not very useful for practical realization of graphene based electronics. Graphene can be synthesized by various methods including micromechanical [31], chemical exfoliation of graphite [44,45], reduction of graphite oxide [46], epitaxial growth on SiC substrate [47,48] and chemical vapor deposition (CVD) on transition metals [49]. Mechanically exfoliated graphene on a  $\text{SiO}_2$  substrate showed its high value of mobility ( $\sim 15,000 \text{ cm}^2/\text{Vs}$ ), offering the possibility of successful operation of FETs in the high frequency region. Although the exfoliation method can be applied to fabricate graphene FET, it cannot be extended for large



**Fig. 2.** (a) Schematic illustration for the measurement of the mechanical properties of free standing monolayer graphene using the AFM tip [56]. (b) Distribution of  $E^{2D}$  derived from a set of measurement [56]. (c) Variation in sheet resistance of graphene that was transferred onto a pre-stretched ( $\sim 12\%$ ) PDMS substrate with respect to uniaxial stretching. Left inset shows the variation in sheet resistance of graphene that was transferred onto an unstretched PDMS substrate [57].

area real practical devices. Many research groups have successfully demonstrated the synthesis of high quality large area graphene using CVD and epitaxial growth [50–52]. This review addresses the electronic and mechanical properties of graphene and exploitation of these excellent properties in fabricating and realizing the graphene based flexible and stretchable FETs.

## 2. Electronic and mechanical properties of graphene

### 2.1. Ultra high mobility in graphene sheet

Graphene is a zero-gap semiconductor, in which charge carriers act as massless Dirac fermions, and that it can show extremely high mobility ( $\sim 200,000 \text{ cm}^2/\text{Vs}$ ) [53]. The carrier concentration in graphene sheet can be continuously tuned from one type to another by applying an ambipolar electric field. Fig. 1a shows the continuous variation of carrier concentration for monolayer graphene by the application of negative and positive biases. The resistivity of the suspended graphene was measured as a function of the gate voltage applied between the graphene and the degenerately doped Si using Hall geometry in vacuum ( $5 \times 10^{-5}$  mtorr) at a low temperature (Fig. 1b [53]). The variation of resistivity as a function of applied gate voltage before (blue) and after current annealing (red) is shown in Fig. 1c. Current annealing of the device was carried out to improve the transport properties of the device; it removes the residual impurities adsorbed on both sides of the graphene surface [54]. The variation in calculated mobility of suspended graphene device as a function of carrier density before (blue) and after (red) annealing is shown in Fig. 1d. The mobility value of the suspended graphene before annealing ( $28,000 \text{ cm}^2/\text{Vs}$ ) was found to be comparable to that of the unsuspended graphene for the same carrier density ( $2 \times 10^{11} \text{ cm}^{-2}$ ). However, after current annealing, the resistance of device decreased by more than 8 times for  $V_g \neq 0$  and the width of Dirac peak reduced by a factor of 20, which indicated improvement in sample quality. Therefore, after current annealing, the decrease in resistance led to the increase in mobility up to  $\sim 230,000 \text{ cm}^2/\text{Vs}$  (Fig. 1d, red line) for carrier density  $2 \times 10^{11} \text{ cm}^{-2}$ . Although graphene has extremely high mobility, the mobility value can be reduced by strong charge carrier scattering. The experimental studies indicated that it is mainly due to the underlying substrate. For example, graphene devices on  $\text{SiO}_2$  show the poor mobility due to charge trapping. Hexagonal boron nitride (h-BN) having an atomically smooth surface offers a solution to avoid this charge trapping effect caused by substrate. Dean et al. fabricated the mechanically exfoliated mono- and Bi-layer graphene devices on single crystal h-BN substrate and demonstrated the ultra high mobility [55]. This ultra high mobility makes the intrinsic graphene a more promising candidate over other existing materials and allows it to be used for fabricating devices that operate at high frequencies. The IBM group exploited the high mobile ability of the charge carrier in graphene and demonstrated wafer-based FETs with a cutoff frequency  $\sim 100 \text{ GHz}$  [56]. Graphene was epitaxially formed by high temperature annealing on a SiC wafer. Ti/Pd/Au (1 nm/20 nm/40 nm) contacts were deposited as source-drain pads. Atomic layer deposited (ALD)  $\text{HfO}_2$  was used as a dielectric layer by using a polymeric buffer layer and Ti/Pd/Au (1 nm/20 nm/40 nm) was again deposited as a top gate. Inset of Fig. 1e shows the schematic cross-sectional image of the top gated graphene FET exhibiting n-type characteristics. The ratio of small-signal drain and gate currents  $|h_{21}|$  (short circuit current gain) derived from the measured scattering (S) parameters and its frequency dependence are shown in Fig. 1e. The cutoff frequency ( $f_t$ ) was 100 GHz for gate length of 240 nm at drain bias of 2.5 V, and was estimated as  $\sim 53 \text{ GHz}$  for gate length of 550 nm. In 2010, Liao et al. demonstrated the intrinsic cutoff frequency up to

300 GHz for graphene transistors [57]. The graphene transistors were fabricated on glass substrate by employing a self-aligned process, a scalable approach, using a CVD grown graphene. The transconductance was recorded as  $0.36 \text{ mS}/\mu\text{m}$  and insulating glass substrate minimizes the parasitic capacitance allowing to achieve the high extrinsic cutoff frequency  $>50 \text{ GHz}$ . Very recently, Guo et al. achieved the maximum oscillation frequency up to 70 GHz in epitaxial graphene transistors fabricated on C-face SiC [58]. They could achieve such high value of frequency by exploiting the high carrier mobility of C-face graphene and using the T-gate structure of device. High carrier mobility provides the low contact resistance between metal and graphene while T-gate structure reduces the gate resistance, particularly in short gate length.

### 2.2. Approaches for non zero gap in graphene sheet

Although graphene shows excellent electronic properties, its gap-less behavior limits its practical use in graphene based electronics, especially where transistors with good on/off ratio is required. There have been few attempts to open the band gap in graphene. Bilayer graphene exhibits inversion symmetry with the AB stacked, which can be broken by application of a transverse electric field [59]. A band gap up to 300 meV can be introduced but introduction of this effect requires a dual gate design, which is not good for industrial applications. Band gap can also be opened in a graphene sheet by patterning the sheet in nanoribbons form because at nanoscale, lattices are no longer approximated as semi-infinite and charge carriers are laterally confined [60]. Recently, graphene nanoribbons (GNR) based transistors showing significant on/off ratios have been fabricated [61–63]. The growth of graphene on a silicon carbide (SiC) substrate introduces a band gap ( $\sim 260 \text{ meV}$ ) because the lattice of SiC matches with graphene and it breaks the sublattice symmetry due to the interaction between graphene and substrate [64]. In addition, the simple way for introducing a gap in graphene is by controlled oxidation of graphene [65]. The complete oxidation of graphene is called graphene oxide (GO) which act as an insulator with a band gap of  $\sim 2.1 \text{ eV}$ . Therefore, the key point is to attach the oxygen atoms with carbon in graphene sheet. It can be done by chemical functionalization of graphene in which oxygen content normally present in carboxyl, hydroxyl or epoxy groups. For this purpose, wet chemical methods gained lot of attention for synthesizing the graphene oxide (GO).

### 2.3. Mechanical properties

#### 2.3.1. Role of flexural mode

The property of graphene to endure high mechanical strains, in addition to its excellent electronic properties, makes it a unique and promising material candidate for flexible electronics. The structural flexibility of a graphene sheet is a direct result of the arrangement and bond formation of its carbon atoms. Carbon atoms in the graphene sheet form the  $\sigma$  bonds resulting in the robust structure. Its carbon-carbon covalent bond, which is the strongest bond in nature, endows graphene with a high Young's modulus and high thermal conductivity. Since graphene is an atomically thin sheet of carbon atoms in 2-dimensional plane, therefore, phonon corresponding to its out-of-plane vibration exist that soften the graphene sheet. Because of these flexural modes, graphene has bendability and lacks a long range structural order, which leads to its crumpling behavior.

#### 2.3.2. Elastic measurement of graphene

The elastic properties of free standing monolayer graphene have been demonstrated using nanoidentation in atomic force microscopy (AFM) [66]. In this demonstration, a sample was

fabricated with the creation of an array of circular wells on a Si substrate coated with 300 nm SiO<sub>2</sub>. Two kinds of wells with diameters 1.5  $\mu\text{m}$  and 1  $\mu\text{m}$  and depth of 500 nm were defined by lithography and reactive ion etching methods. For the measurement of the mechanical properties of free standing monolayer graphene, the centers of the circular wells were indented by the AFM tip, as shown in Fig. 2a. The force–displacement behavior of suspended graphene was investigated with respect to nonlinear elastic stress–strain response, and elastic constant ( $E^{2D}$ ) and breaking strength were determined. To obtain statistical data, graphene membranes of two different graphene flakes, were made over the array of circular wells. For each membrane, loading/unloading measurement was repeated three times. The distribution of  $E^{2D}$  derived from a set of measurement is shown in Fig. 2b, where the mean value of  $E^{2D}$  is  $\sim 342 \text{ N m}^{-1}$  with a standard deviation of  $30 \text{ N m}^{-1}$ . The breaking strength was determined to be  $\sim 42 \text{ N m}^{-1}$ , representing the intrinsic strength of a defect-free sheet. These quantities corresponded to the Young's modulus of  $\sim 1 \text{ Tpa}$ , indicating the excellent mechanical properties of intrinsic graphene.

### 2.3.3. Stretching ability of graphene

To further investigate the mechanical endurance of graphene for the realization of flexible/stretchable applications, a large area graphene film was grown and its electrical properties and stretching ability were demonstrated [67]. High quality, large area graphene films, exhibiting low sheet resistance of  $\sim 280 \Omega$  per square with 80% optical transparency, were grown on a thin Ni layer by chemical vapor deposition (CVD) method. After the growth process, these graphene films were easily transferred to arbitrary substrates. For measuring the sheet resistance under stretching, the graphene films were transferred to unstretched and pre-stretched PDMS substrates. Fig. 2c shows the variation in sheet resistance of graphene that was transferred onto a pre-stretched ( $\sim 12\%$ ) PDMS substrate with respect to uniaxial stretching. The left inset of Fig. 2c shows the variation in sheet resistance of graphene that was transferred onto an unstretched PDMS substrate. The graphene film on the unstretched PDMS substrate showed good recovery of sheet resistance after 6% stretching, beyond which mechanical failure started. To improve the stretchability of graphene, graphene films were transferred onto a pre-stretched PDMS. The graphene film on the longitudinally pre-stretched PDMS did not show much improvement in sheet resistance due to the transverse strain induced by Poisson's effect, whereas that on the isotropically pre-stretched (up to  $\sim 12\%$ ) PDMS substrate showed stable sheet resistance up to  $\sim 11\%$  in both longitudinal and transverse ( $R_x$  and  $R_y$ ) directions. Only one order of change in sheet resistance was observed up to  $\sim 25\%$  stretching. In addition, Bae et al. demonstrated the synthesis of large area 30 in. graphene by employing the roll-to-roll fabrication method [49]. The synthesized graphene film showed the excellent stretching ability ( $\sim 6\%$ ) without changing the sheet resistance whereas ITO suffers serious increase of sheet resistance after  $\sim 2.5\%$ .

## 3. Flexible field effect transistor: A perspective for digital/logic applications

Graphene can be used as an active layer and electrodes in FETs, and as an electrode in solar cells and organic lighting emitting diode (OLED) which require good transparency as well as good conductivity. Here, the recent development of graphene based FETs in exploring the potentiality of graphene based electronic in flexible and stretchable format are addressed.

### 3.1. Graphene with conventionally available inorganic materials

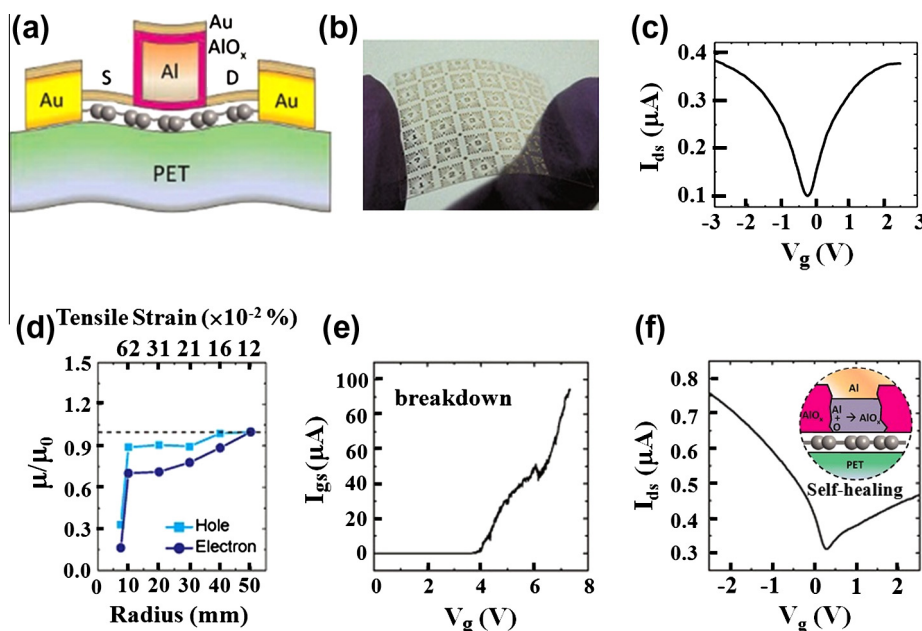
The FETs is a key component of microelectronics. Numerous reports on graphene based FETs address various issues related to device structure and selection of materials compatible to flexibility and stretchability. Fig. 3 shows the performance of a flexible graphene FET exhibiting high mobility with a self healing gate dielectric [68]. Fig. 3a shows the schematics cross-section of the device structure. Graphene was synthesized by the well known CVD method on a Cu foil, followed by a wet transfer process using Poly(methyl Methacrylate) (PMMA) as the supporting layer. Graphene strip, as a channel, was defined by e-beam lithography and undesired graphene was etched out by O<sub>2</sub> plasma. Source–Drain electrodes (0.5 nm Cr/60 nm Au) and top gate (Al, 70 nm) were defined by e-beam lithography, followed by metal deposition using thermal evaporation. The advantage of Al deposition as top gate is that no additional gate dielectric deposition between graphene and Al is required. After Al deposition, the device was exposed to air for 6 h allowing the oxidation of the Al surface, which forms the thin AlO<sub>x</sub> film acting as a gate dielectric. Another layer of Cr (0.5 nm)/Au (10 nm) was deposited, which was automatically aligned by Al/AlO<sub>x</sub> such that the source–drain electrodes were separated. Fig. 3b shows the array of such TFTs on the bendable poly(ethylene terephthalate) (PET). The FETs exhibited good ambipolar behavior and a charge neutrality point near to zero volt, as shown in Fig. 3c. Little deviation from the zero gate voltage is due to unintentional electron doping. The electron and hole mobilities were 230 and 300 cm<sup>2</sup>/V s, respectively, and the on/off ratio was in the range  $\sim 3$ –6. The variation of normalized mobility as a function of tensile strain and bending radius is shown in Fig. 3d, indicating stable electrical performance of the FETs up to the bending radius of  $\sim 8 \text{ mm}$ . The most important advantage of this device structure and selected material is that the gate dielectric can be self-healed by electrical annealing or by several hours of air exposure, in response to a pin hole and nano fracture that can be produced in the gate dielectric by multiple bending. To verify this self-healing, the dielectric layer was intentionally broken by increasing the gate–source voltage beyond the breakdown field. After the breakdown of the dielectric layer, leakage current was increased abruptly as shown in Fig. 3e. Normally, a dielectric layer breaks at the thinnest part and the ambipolar behavior of the FET disappears due to the loss of potential modulation by the sweeping gate voltage. Upon exposure of the device to air for 6 h, the native oxide near the damaged areas reformed. During the air exposure, H<sub>2</sub>O or O<sub>2</sub> diffused (inset of Fig. 3f) at the graphene/Al interface to promote the re-growth of the damaged area. After the dielectric layer self-healed, the FET showed a v-shaped transfer curve (Fig. 3f), indicating regained device performance.

In the above described report, graphene was used for the channel, and conventionally available materials were used for the source–drain electrodes, gate dielectric and gate electrode. It has been expected and realized that materials more compatible to flexibility and stretchability can be printed and processed more easily than conventionally available inorganic materials.

### 3.2. Graphene with compatible active layer materials: Search for printable gate dielectric

Conventionally available inorganic materials are brittle because of poor endurance against external strain. Therefore, it is desirable to use the new materials which could show good compatibility in flexible format together with maintaining the FET performance. Gate dielectric plays a crucial role in getting a good performance of FET as its interface to the channel strongly controls the output current with the sweeping voltage. In the flexible context, we can easily think about the organic/polymeric materials which are





**Fig. 3.** (a) Schematics representation of cross-section of the flexible graphene FET on PET substrate with a self healing gate dielectric. (b) Photograph of the array of such TFTs on the PET showing its flexibility. (c) Shows a good ambipolar behavior and a charge neutrality point near to zero volt of graphene FET. (d) Variation of normalized mobility as a function of tensile strain and bending radius indicating stable electrical performance of the FETs up to the bending radius of  $\sim 8$  mm. (e) Variation of leakage current after the breakdown of the dielectric layer showing its abrupt increase. (f) The performance of FET showing a v-shaped transfer curve after self healing of the dielectric layer indicating regaining ability of device. Inset shows the diffusion of H<sub>2</sub>O or O<sub>2</sub> at the graphene/Al interface to promote the re-growth of the damaged area during the air exposure [68].

obviously low temperature processable, easy printable and having good mechanical endurance against external strain as compared to conventionally available inorganic materials.

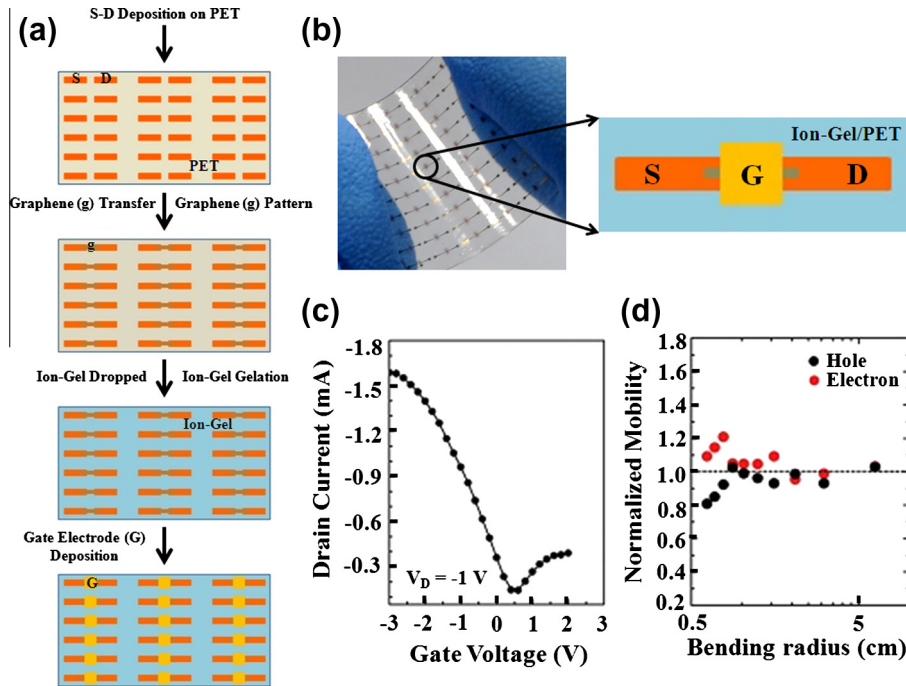
### 3.2.1. Solid polymer electrolyte: Ion-gel gate dielectric

Solid polymer electrolyte in which the salt dissolved in polymer matrix is one of potential candidates for gate dielectric with easy printing ability. Polymer electrolyte often results in high capacitance as high polarization can easily be achieved by virtue of mobile ions. Cho et al. [69] demonstrated the high capacitive solid polymer electrolytes which is known as ion-gel. Ion-gel showed a specific capacitance up to  $\sim 10$  μF/cm<sup>2</sup> at 10 kHz.

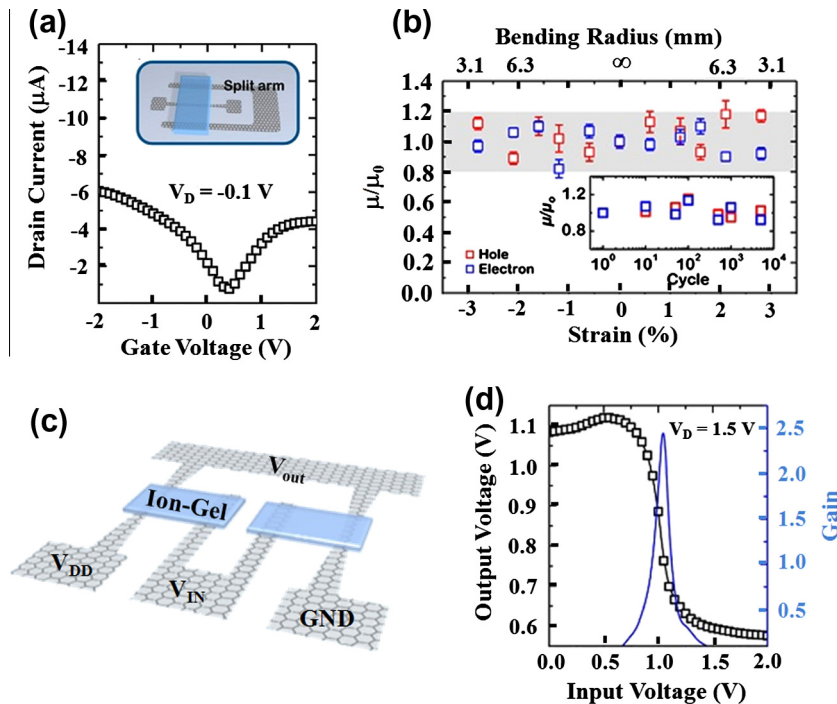
**3.2.1.1. Graphene FET with ion-gel: Conventional structure.** A solution processable, high capacitive and easily printable, ion-gel was used as a gate dielectric in fabricating graphene based flexible FETs [70]. Ion-gel is a mixture of ionic liquid and triblock copolymer, which gels the ionic liquid. It exhibits high capacitance, which gives the graphene FETs their high on-currents and low operating range. In addition, it is in gel form which has a good mechanical endurance. Fig. 4a shows the fabrication steps of an ion-gel gated graphene FET array on a PET substrate. First, source-drain electrodes (Cr/Au) were deposited on the PET substrate, and after that, a graphene film was transferred onto the substrate using PMMA polymer as the supporting layer. A graphene channel was defined by photolithography and reactive ion etching (RIE) methods. The ion-gel was prepared by mixing poly(styrene-block-methyl-methacrylate-block-styrene) (PS-PMMA-PS) triblock copolymer and 1-ethyl-3-methylimidazolium bis(tri-methylfluorosulfonyl)imide ([EMIM][TFSI]) ionic liquid in methylene chloride at a 0.7:9.3:90 ratio. The prepared ion-gel was drop-casted on patterned graphene, and a top gate electrode (Au) was thermally deposited using a shadow mask. Fig. 4b shows the ion-gel gated graphene FET array on PET in bending form, showing the FET's flexibility. The transfer curve of the graphene FET on the PET substrate with the ion-gel gate dielectric is shown in Fig. 4c. The transfer curve reveals that

the FET operated in the low voltage region ( $\pm 3$  V) with the Dirac point at  $\sim 0$  V and at high on-current. In case of the SiO<sub>2</sub> gate dielectric, the operating region of graphene FET was observed within  $\pm 40$  V with the Dirac point at  $\sim +40$  V. The capacitance of the ion-gel was ( $\sim 5.17$  μF/cm<sup>2</sup>), which is higher than the 300 nm thick SiO<sub>2</sub> at 10 Hz. The high capacitance of the ion-gel was due to the formation of the electric double layer at the ion-gel/graphene and ion-gel/gate electrode interfaces; it resulted in the operation of the FET in the low voltage region. The average hole and electron mobilities of the FET with the ion-gel gate dielectric on the PET were  $\sim 203 \pm 57$  and  $91 \pm 50$  cm<sup>2</sup>/V s, respectively, and those of the graphene FET on a Si substrate with a SiO<sub>2</sub> gate dielectric were  $\sim 828 \pm 58$  and  $189 \pm 42$  cm<sup>2</sup>/V s, respectively. It was assumed that the carrier mobilities using the ion-gel gate dielectric were lower than those using the SiO<sub>2</sub> dielectric because the graphene/ion-gel interface was rougher than the graphene/SiO<sub>2</sub> interface. The variation of the normalized electron-hole mobility with respect to the bending radius is shown in Fig. 4d. Carrier mobility decreases by 20% of its initial value as the bending radius changes from 6 cm to 0.6 cm.

**3.2.1.2. Graphene FET with ion-gel: Co-planar structure.** Kim et al. [71] demonstrated transparent, flexible graphene based FETs by adopting a more simplified device structure using a co-planar gate, channel and source-drain. The advantage of this structure is that it simplifies the fabrication steps with one-step patterning of the channel and gate electrodes. A schematic of a graphene FET in a coplanar gate configuration is shown in the inset of Fig. 5a. Ion-gel exhibits long range ordering polarizability, which keeps the gate electrode (split arms) offset to the channel (main strip). The region of the graphene main strip in contact with the ion-gel can only act as a channel and its conductivity can be tuned by applying a bias voltage at the split arms. The uncovered regions of the graphene main strip with ion-gel at both ends form the source-drain electrodes. The overall transparency of the complete device with the PET substrate was estimated to be  $\sim 84\%$ . A large drain current



**Fig. 4.** (a) Schematic illustration of various key steps in the fabrication of an ion-gel gated graphene FET array on a PET substrate. (b) Photograph of the ion-gel gated graphene FET array on PET showing its bendability and zoom part shows the schematic of single FET. (c) Transfer curve of the ion-gel gated graphene FET on the PET substrate. (d) Variation of the normalized electron-hole mobility with respect to the bending radius [70].



**Fig. 5.** (a) Variation of the drain current as a function of the gate voltage showing the V-shaped ambipolar behavior in the low operating region ( $\pm 2$  V). Inset shows the schematic of a graphene FET in a coplanar gate configuration. (b) Shows the variation of the normalized mobilities of electrons and holes with respect bending radius and their corresponding strain values. Inset shows the mobility variation with respect to bending cycles up to 5000 and maximum strain of  $\sim 2\%$  experienced by the device during one cycle. (c) Schematic illustration of the fabricated inverter in which two coplanar gated FETs are connected. (d) Shows the inverting characteristic as well as the plotted gain at  $V_{DD} \sim 1.5$  V for the coplanar gated FET arranged in the inverting configuration [71].

( $I_d$ )  $\sim 30 \mu$ A was observed at low drain voltage ( $V_d$ ) of  $\sim 0.5$  V and gate voltage ( $V_g$ ) of  $\sim -2$  V. Fig. 5a shows the variation of the drain current as a function of the gate voltage, clearly showing the V-shaped ambipolar behavior in the low operating region ( $\pm 2$  V).

The positive and negative gate regions represent the electron and hole transport, and a charge neutrality point was observed near  $\sim 0$  V. The low operating region and Dirac point near zero voltage are due to the large capacitance of ion-gel, which is calculated as

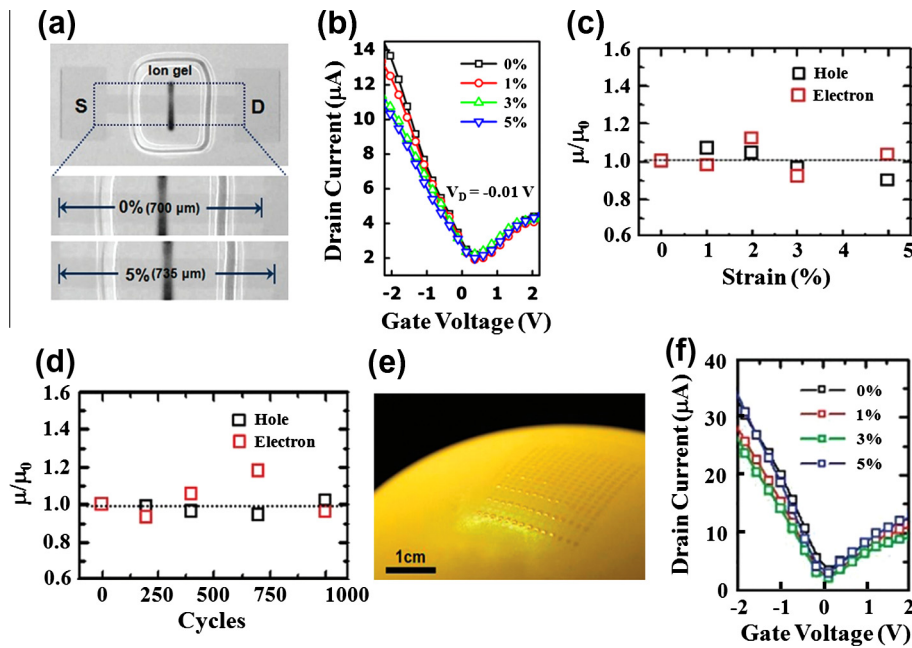
$\sim 8.1 \mu\text{F}/\text{cm}^2$  in metal/insulator/metal coplanar electrode structure. The calculation of mobility in the coplanar structure is slightly different from that of mobility in the conventional structure. In the coplanar structure, the resistivity of the source–drain electrodes (contributed by the main strip region which is not covered by ion-gel) becomes higher than that of the channel (the region covered by ion-gel) when the FET is on. To calculate the channel resistance accurately, electrodes resistance were subtracted from the total resistance and mobility was calculated. The average hole and electron mobilities of the coplanar gated graphene based FET were estimated to be  $\sim 892 \pm 196$  and  $628 \pm 146 \text{ cm}^2/\text{V s}$  respectively. The mechanical flexibility and robustness of devices were investigated by bending tests in forward and backward directions. Fig. 5b shows the variation of the normalized mobilities of electrons and holes with respect to bending radius and their corresponding strain values; the maximum change in mobility is  $\sim 20\%$  within the strain of 2.8%. The inset of Fig. 5b shows the mobility variation with respect to bending cycles up to 5000 and maximum strain of  $\sim 2\%$ . The maximum change in mobility during repeated cyclic tests was found to be within 20%. This indicates that the device showed the good reliability and stable performance during mechanical deformation. By taking advantage of the simplified coplanar FET structure, a complementary graphene based inverter was fabricated on a PET substrate. Fig. 5c shows the schematics of the fabricated inverter, in which two coplanar gated FETs are connected. Both the transistor share a common input ( $V_{\text{IN}}$ ) and output ( $V_{\text{OUT}}$ ) and the supply voltage ( $V_{\text{DD}}$ ) is applied to one transistor while other is grounded (GND). For a single graphene FET, the Dirac point shifted as a function of drain voltage. In the inverter configuration, the two identical FETs showed different Dirac points depending on the distribution of the supply voltage across them during the sweeping of the input voltage ( $V_{\text{IN}}$ ), which as a result, lead to the inverter characteristics. Fig. 5d shows the inverting characteristic as well as the plotted gain at  $V_{\text{DD}} \sim 1.5 \text{ V}$  for the coplanar gated FET arranged in the inverting configuration. The maximum gain of the inverter in this coplanar configuration is calculated to be  $\sim 2.6$ .

**3.2.1.3. Integration of stretchability.** In addition to the flexibility, stretchability is also needed in graphene based FETs for practical realization of conformal and wearable devices. Lee et al. carried out significant investigations with respect to stretchability, demonstrating a graphene based FET with ion-gel gate dielectric on a stretchable substrate by transfer and aerosol printing methods with low temperature processing [72]. The graphene patterned directly on Cu foil was transferred onto a rubber-like substrate. An ion-gel gate dielectric was printed by the aerosol jet printing method having printing resolution of  $\sim 50 \mu\text{m}$ . A poly(3,4-ethylenedioxythiophene) oxidized with poly(4-styrenesulfonate) (PEDOT:PSS) was printed as a gate electrode by covering the channel region. The use of ion-gel as a gate dielectric enables the quick formation of an electric double layer, regardless of the area of overlap between the gate electrode and the active channel region as it relies on the motion of the mobile ions. Initially, the FET was fabricated using monolayer graphene in the channel region, which showed the V-shaped ambipolar behavior at  $V_D = -0.1 \text{ V}$ . The average hole and electron mobilities were estimated to be  $\sim 26$  and  $20 \text{ cm}^2/\text{V s}$ , respectively. The low value of mobility in the monolayer graphene based FET was due to scattering from the molecular species inside the porous structure of the PDMS and to exposure of graphene devices to contaminating species, which reduced the transport of carriers in graphene. To overcome these effects, bi- and tri-layer graphene channels were used to fabricate the FET. The advantage of using bi- or tri-layer graphene as a channel is that the bottom layer provides sufficient screening of charges species in the porous structure of the PDMS and that the top layer suppresses

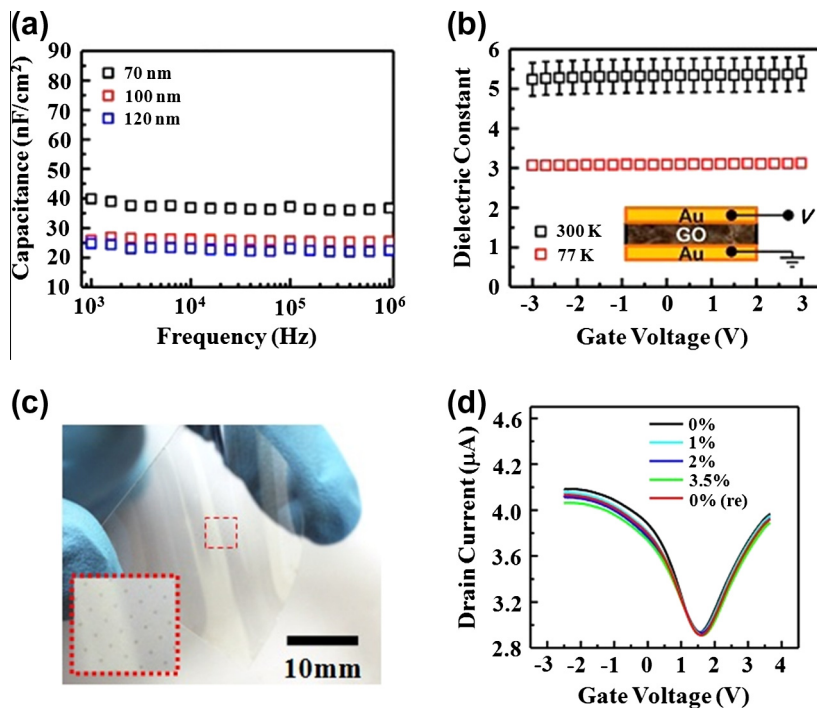
the effect of environmental contamination like moisture and other adsorbing species. Therefore, the hole and electron mobilities increase with the number of graphene layers and were estimated to be  $\sim 1131 \pm 31$  and  $362 \pm 45 \text{ cm}^2/\text{V s}$  for the tri-layer graphene channel, respectively. The electrical performance of the tri-layer graphene based FET was measured under a stretching test. Fig. 6a shows the optical microscopic image of the FET with (up to 5%) and without stretching. The ambipolar behavior of the graphene FET under stretching within the range of 0–5% indicates its stable operation due to excellent compatibility of graphene and ion-gel to stretching (Fig. 6b). The variations of hole and electron normalized mobilities with respect to stretching and the number of repeated cycles are shown in Fig. 6c and d, respectively. The change in the hole and the electron mobility during stretching is less than 15%, indicating the good stretchability of the FET. Under repeated cyclic tests, the electrical properties of the device were found to be invariant even after 100 cycles with 3% stretching in each cycle. During the measurement, it was observed that the maximum hole and electron currents and the minimum current at Dirac voltage were independent of stretching and the cyclic tests. This excellent mechanical endurance has allowed the fabrication of such devices on highly compliant substrates such as ultrathin plastic or rubber substrates. Graphene FETs were fabricated on balloons, as shown in Fig. 6e and their electrical performances under stretching were investigated. Fig. 6f shows the transfer characteristics of the graphene FETs on the balloons with uniaxial stretching during the inflation of the balloons. The graphene FETs on the balloons showed good electrical performance without any significant change under stretching, revealing that a graphene based FET together with an ion-gel gate dielectric can be used to fabricate stretchable electronics without including a special design like a wave or buckling in electronic circuitry.

### 3.2.2. Graphene oxide gate dielectric

Graphene oxide (GO) which can be derived by the oxidation of graphene is recently realized as a suitable gate dielectric for graphene in the similar way as  $\text{SiO}_2$  gate insulator for Si semiconductor. GO can be prepared by a solution process and can easily be applied to a graphene channel as a gate dielectric. Lee et al. demonstrated an all graphene-based transistor on a plastic substrate by employing GO as a gate dielectric and graphene as a channel, S–D and gate electrodes [73]. GO flakes were stabilized in aqueous phase by negatively charged functionalities and an immiscible water/oil interface was formed by pouring hexane on the water surface. Then, ethanol was added slowly to trap the GO flakes at the interface. The ethanol suppressed the surface charges on the GO flakes and adsorbed the GO flakes at the interface to reduce the interface energy at the water/hexane interface. Hexane was evaporated to leave the 2-D GO flakes floating on the water surface. The floating GO flakes were then lifted off and transferred onto the desired substrate many times to obtain a pin hole free GO film. This method is called the Langmuir–Blodgett (LB) method. To confirm the suitability of GO as a gate material, the insulating and dielectric properties of GO were investigated. The leakage current density of the GO film was estimated to be  $\sim 17 \text{ mA}/\text{cm}^2$  at the bias field of  $\sim 50 \text{ mV}/\text{cm}$  with application of voltage between the top and bottom electrodes. The current through the GO film was found to be unstable when the bias voltage exceeded 15 V, at which the electric field  $\sim 1.5 \times 10^6 \text{ V}/\text{cm}$  breaks down. Fig. 7a shows the variation of capacitance for different thicknesses of the GO film normalized to  $1 \text{ cm}^2$  as a function of frequency from 1 kHz to 1 MHz at 77 K. The capacitance of the GO film for different thickness was found to be very stable without any dielectric dispersion up to 1 MHz. The variation of the dielectric constant of the GO film with respect to the gate voltage at different temperatures is shown in Fig. 7b. The dielectric constant at 77 K was estimated to be  $\sim 3.1$ , but it



**Fig. 6.** (a) Shows the optical microscopic image of the FET with (up to 5%) and without stretching. (b) Ambipolar behavior of the graphene FET under stretching within the range of 0–5%, indicating its stable operation due to excellent compatibility of graphene and ion-gel to stretching. Variations of normalized mobilities of hole and electron with respect to (c) stretching and the (d) number of repeated cycles, respectively. (e) Photograph of graphene FETs fabricated on balloons. (f) Transfer characteristics of the graphene FETs on the balloons with uniaxial stretching during the inflation of the balloon [72].



**Fig. 7.** (a) Shows the variation of capacitance for different thicknesses of the GO film normalized to 1 cm<sup>2</sup> as a function of frequency from 1 kHz to 1 MHz at 77 K. (b) Variation of the dielectric constant of the GO film with respect to the gate voltage at different temperatures. (c) Photograph of graphene based FET array with 100 nm GO gate dielectric on a PET substrate. (d) Shows the V-shaped ambipolar behavior of the FET for different strain values based on different bending radii [73].

increases up to  $\sim 5$  at room temperature. The capacitance and dielectric value exhibited by the GO film seemed reasonable for use of the GO film as a gate dielectric in a graphene based FET. A graphene based FET with 100 nm GO gate dielectric was fabricated on a PET substrate and the photograph of the complete device is shown in Fig. 7c. Fig. 7d shows the V-shaped ambipolar behavior

of the FET for different strain values based on different bending radii. The FET showed hole and electron mobilities of  $\sim 150$  and  $116$  cm<sup>2</sup>/V s, respectively. The device showed a very well repeated V-shaped transfer curve for different bending radii and even after recovery, representing the excellent mechanical robustness of a graphene based FET with a GO gate dielectric.



The above reviewed recent work mainly focused on the development of graphene based FETs in flexible format showing poor on/off ratio which does not fulfill the requirement for the potential use of these FETs in digital applications. For realizing the graphene based digital/logic applications it is quite important to open the band gap in graphene (see Section 2.2).

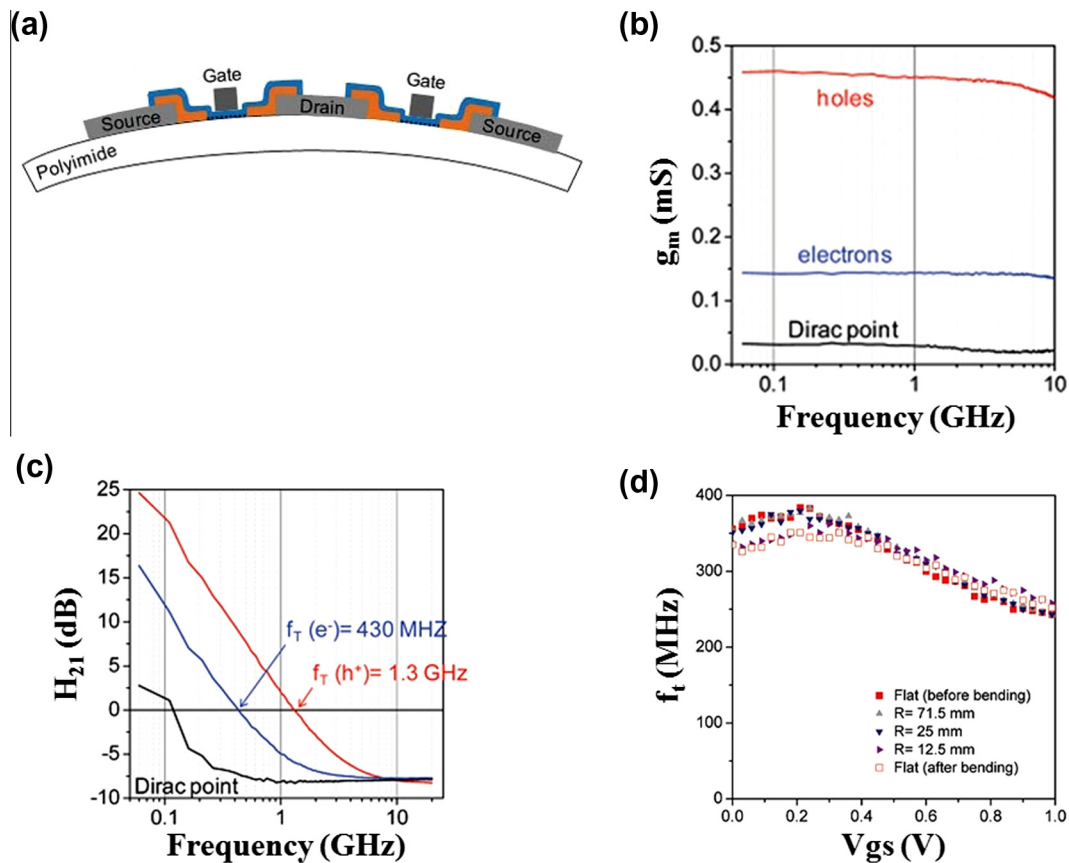
#### 4. High frequency flexible field effect transistor: A perspective for analogue/radio frequency applications

Zero band gap of graphene is the main hurdle in fabricating the graphene based digital applications. On the other hand, its ultra high mobility, current carrying capacity and saturation velocity offer the fabrication of radio frequencies (r.f.) electronic devices where a large on/off ratio in FET is not necessary. In this context, several groups have been demonstrated the high frequency graphene based FET [56,74,75]. The fabrication of graphene based r.f. devices is also demanding for realizing the real applications of plastic electronics. Recently, few attempts have been taken in this direction using CVD grown graphene as well as solution based graphene.

##### 4.1. Solution based single layer graphene for flexible gigahertz transistor

Sire et al. [37] demonstrated the flexible FET by employing the solution based isolation of single layer graphene flakes via density gradient ultracentrifugation (DGU) which can operate in gigahertz

frequencies region. Fig. 8a shows the schematic illustration of two graphene based FETs in ground-signal-ground (GSG) configuration for r.f. measurement. The dimensions of the device were defined as distance between source and drain  $\sim 260$  nm, gate length  $\sim 170$  nm and gate width  $\sim 40$   $\mu\text{m}$ . 20 nm of yttrium oxide was used as a gate dielectric which was grown by four successive depositions of 3 nm thick yttrium film followed by 10 min exposure of oxygen. The value of  $V_{\text{gs}}$  was optimized to get the highest value of r.f. transconductance ( $g_m$ ) and current gain for hole and electron. The variation of  $g_m$  for electrons, holes and near to Dirac point (close to zero) is almost constant up to 5 GHz as shown in Fig. 8b. The variation of current gain ( $H_{21}$ ) with respect to frequencies is shown in Fig. 8c which indicates that the cutoff frequencies ( $f_t$ ) for holes and electrons were observed as 1.3 GHz and 430 MHz (at  $V_{\text{ds}} = -0.6$  V) and the value of  $H_{21}$  near Dirac point is almost negative i.e. low transconductance at this region. Further increment in cutoff frequency for holes (up to 2.2 GHz, at  $V_{\text{gs}} = -0.6$  V and  $V_{\text{ds}} = -0.65$  V) was observed in this device by performing the vacuum annealing. In de-embedding case, the intrinsic cutoff frequency was estimated up to 8.7 GHz. Another important feature, power gain cutoff frequency ( $f_{\text{max}}$ ) which is not as sensitive as  $f_t$ , and more reliable, was estimated to be 550 MHz. The performance of this graphene based r.f. device in flexible format was also tested. Fig. 8d shows the variation of  $f_t$  with respect to  $V_{\text{gs}}$  before bending, with bending ( $r = 71.5$  mm, 25 mm, 12.5 mm) and after relaxing the bending. It has been observed that up to 25 mm bending radius,  $f_t$  did not change significantly but at higher bending radius,  $V_{\text{gs}}$  value was shifted and device showed degraded irreversible performance. The irreversible, degraded performance was attributed



**Fig. 8.** (a) Schematic cross-section of the flexible graphene FET in GSG configuration. (b) Variation of transconductance as a function of frequency for electrons, holes and near to Dirac point (close to zero) indicating its almost constant value up to 5 GHz measured at  $V_{\text{gs}} = -1$  V ( $I_d = -9.68$  mA) for holes (red) and  $V_{\text{gs}} = 1$  V ( $I_d = -8.39$  mA) for electrons (blue) and at the Dirac point (black). (c) Variation of current gain ( $H_{21}$ ) with respect to frequencies showing the cutoff frequencies for electrons and holes. (d) Variation of  $f_t$  with respect to  $V_{\text{gs}}$  before bending, with bending ( $r = 71.5$  mm, 25 mm, 12.5 mm) and after relaxing the bending [37]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

to poor contact of graphene flakes that connections become loose upon bending.

#### 4.2. CVD grown graphene based flexible gigahertz transistor

Recently, Petrone et al. exploited the CVD grown graphene by taking the advantage of its uniform large size over solution based flakes connected graphene one and demonstrated the unity current gain frequencies ( $f_t$ ) and unity power gain frequencies ( $f_{max}$ ) in gigahertz range using CVD grown graphene based FET [76]. The device was fabricated on polyethylene naphthalate (PEN) substrate in bottom gate configuration with atomic layer deposited 6 nm thick  $\text{HfO}_2$  gate dielectric. The dimensions of the FET were defined as gate length of  $\sim 500$  nm, channel length of  $\sim 900$  nm and channel width of  $\sim 15$   $\mu\text{m}$ . The S-parameters were measured and extracted current gain ( $H_{21}$ ) and unilateral power gain (U) with respect to frequencies for without (0%) and with bending (1.75%) are shown in Fig. 9a and b respectively. The value of S-parameters was measured at  $V_{ds} = 0.5$  V and  $V_{gs}$  value was optimized to get the maximum transconductance, however, these values were changed with bending as Dirac point shifted with bending response. The  $f_t$  and  $f_{max}$  values at 0% strain were measured as 7.2 GHz and 2.6 GHz at  $V_{gs} = -0.25$  V (Fig. 9a). The performance of the device at 1.75% strain (Fig. 9b) were found to be almost similar as for unstrained. Fig. 9c–e show the normalized behavior of relevant device parameters such as mobility ( $\mu_{FE}$ ),  $f_t$  and  $f_{max}$  to unstrained. The maximum variance in  $\mu_{FE}$  was  $\pm 30\%$  up to 1.75% strain and in  $f_t$  and  $f_{max}$  were  $\pm 20\%$  up to 1.1% strain values. The values of  $V_{gs}$  corresponding to different strain points are shown in Fig. 9d. This work is a first demonstration showing the operation in GHz regime at strain above 0.5% which is significant improvement towards graphene based flexible r.f. applications.

#### 4.3. Flexible quaternary digital modulation: All graphene based circuits

An approach has been attempted in fabricating the graphene based flexible modulator in the context of flexible wireless

communication applications [77]. The fabricated flexible modulator can encode the two bits of information per symbol and each component of circuit including transistor channels, the interconnects between transistors, load resistance, source/drain/gate electrodes—all were fabricated with graphene owing to flexibility and transparency. Fig. 10a shows the schematics of all graphene based devices fabricated on flexible PEN substrate. The top and bottom layers form top and bottom gate while middle layer forms the channel and interconnects. All these three layers were isolated by atomically layer deposited dielectric. The overall transparency was found to be more than 93% as in most of area was covered by monolayer graphene. The fabricated modulator circuit was tested under mechanical strain. The ratio of two peaks at  $\omega$  and  $2\omega$  corresponding to original and doubled frequency represents the spectral purity of frequency doubling which is plotted with different bending radii and shown in Fig. 10b. Fig. 10c shows the plots of various binary and quaternary modulation schemes such as binary amplitude shift keying (BASK) (black), binary phase shift keying (BPSK) (red), binary frequency shift keying (BFSK) (blue) and quaternary amplitude shift keying (4-ASK) (green) under bending radius of 5.5 mm (2.7% strain). The output results of all these modulation schemes in time domain revealed that the graphene based flexible and transparent modulation circuits has good compatibility in flexible format. This demonstration revealed that the graphene can be future material for realizing the flexible r.f. applications.

#### 5. Summary and outlook

Review on recent development of graphene based FETs concludes that graphene can be considered as a good candidate for flexible electronics. It can be used as electrodes (source and drain) as well as a channel layer in any kind of FET structure. The important thing is to search a high capacitive, easy printable, durable and compatible material for gate dielectric. In terms of high capacity and easy printability, polymer electrolyte can be one of good materials but its slow response with frequency hinders to achieve the good performance of TFT. GO can be a good insulator, considering

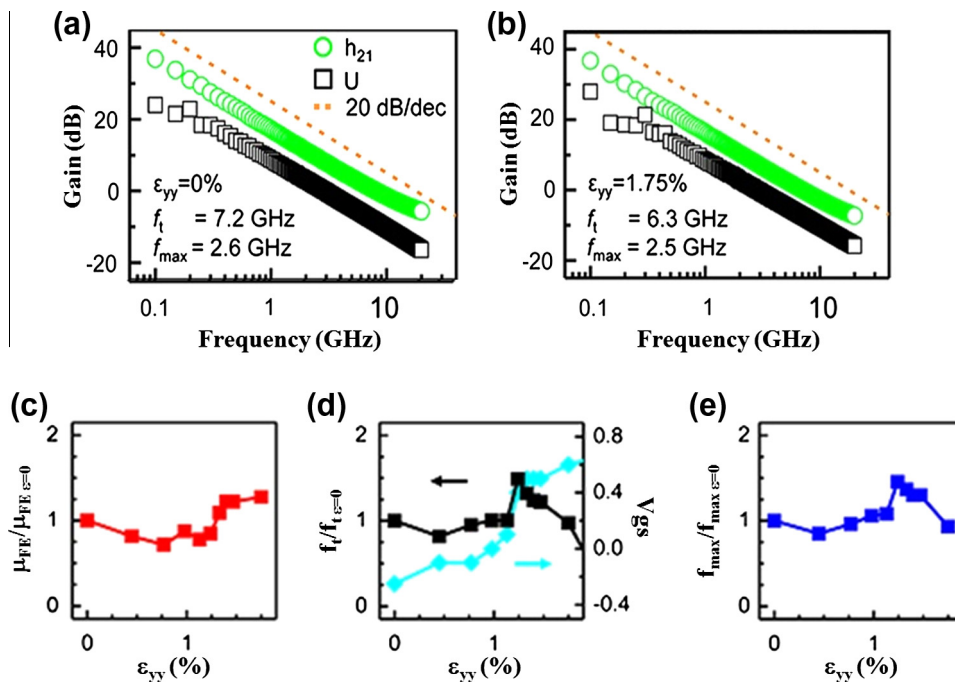
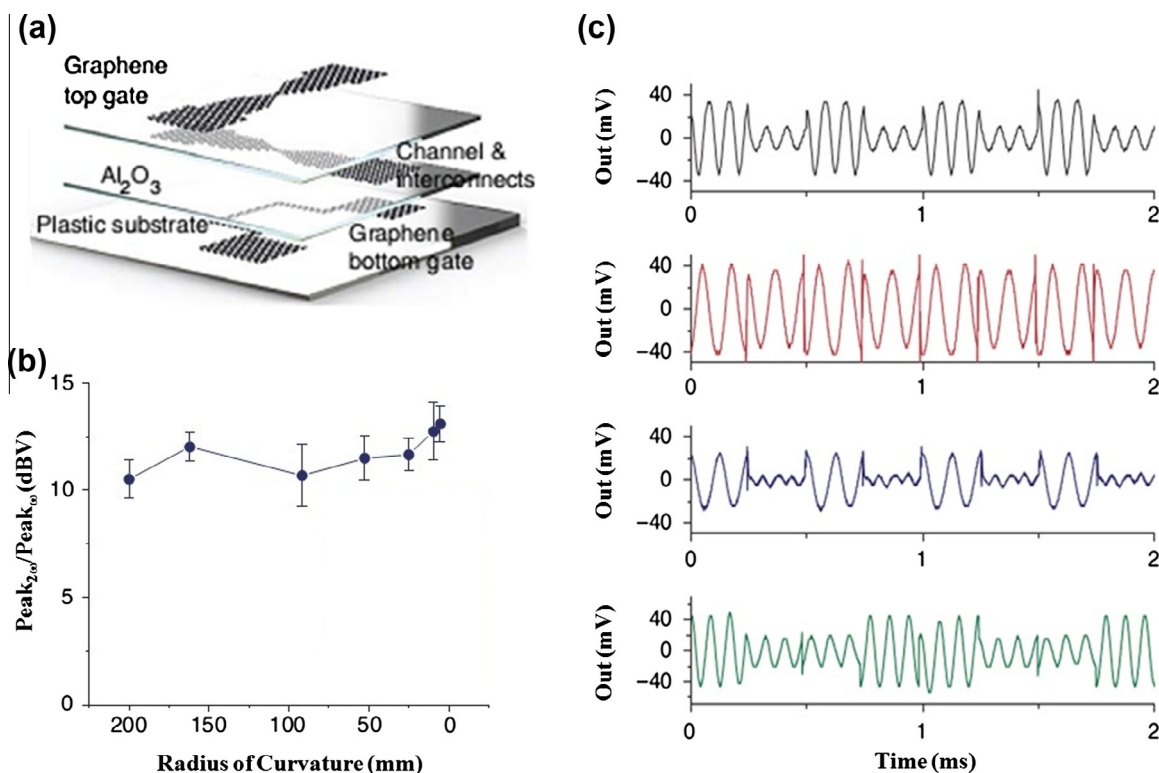


Fig. 9. The plot of current gain ( $H_{21}$ ) and unilateral power gain (U) extracted from measured S-parameters with respect to frequencies for (a) without (0%) and (b) with bending (1.75%). The normalized behavior to unstrained for (c) mobility ( $\mu_{FE}$ ), (d)  $f_t$  and (e)  $f_{max}$  with respect to strain [76].



**Fig. 10.** (a) The schematics of all graphene devices fabricated on flexible PEN substrate. (b) Variation of the signal amplitude ratio of the original and the doubled frequency with respect to radius of curvature for a graphene frequency doubler. (c) Plots of various binary and quaternary modulation schemes: BASK (black), BPSK (red), BFSK (blue) and 4-ASK (green) under bending radius of 5.5 mm (2.7% strain) [77]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

compatibility with graphene, but the formation of high quality GO film is required. Graphene has great advantage for flexible electronics but at the same it needs an opening of band gap for digital applications. In this regard, organic material based FETs are of much attractive as they can easily be fabricated by printing method and exhibit good on/off ratio. For the past 10 years, numerous reports on organic field effect transistor in flexible format have been demonstrated [78,79]. Recently Yi et al. fabricated the solution processable organic FET on thin plastic sheet wherein flexibility could be achieved up to the bending radius as small as  $\sim 200 \mu\text{m}$  with the maintaining of electrical performance [80]. In addition, Sekitani et al. successfully fabricated the organic based FETs and complementary circuit where the folding radius was achieved up to  $\sim 100 \mu\text{m}$ , exhibiting the mobility of  $\sim 0.5 \text{ cm}^2/\text{Vs}$  which is comparable to the amorphous Si TFT at low operating voltage of  $\sim 2 \text{ V}$  [81]. Further, they also demonstrated large area stretchable electronics enabled by organic FET arrays [82]. For such electronic applications where FETs need both good on/off ratio and high flexibility, organic semiconductor looks superior over graphene. However, the main obstacles with organic materials are their low mobility and degradation with time as these are highly sensitive to environment moisture and processing. So presently both graphene as well as organic semiconductor based FETs have been become a subject of intense research as in some aspects graphene is superior over organic materials and vice versa. Researchers had tried to get the good on/off ratio in graphene based FETs by fabricating the GNR as a channel layer. However there are various issues evolve in fabricating the GNR based FETs. For example, nanoribbon has rough edges creating more scattering to the carriers. The other issue is that substrate induces the disorder on which nanoribbons are fabricated. Although graphene needs various technological issues to overcome but it looks promising for flexible

electronic applications which would be difficult to realize with conventional materials.

### Acknowledgements

This work was supported by the Basic Research Program (2012R1A2A1A03006049 and 2009-0083540) through the National Research Foundation of Korea (NRF), funded by the Ministry of Education, Science and Technology and the Technology Innovation Program (Grant 10041066) funded by the Ministry of Knowledge Economy (MKE), Republic of Korea.

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