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FEATURE ARTICLE

Graphene-based flexible and stretchable thin film transistors

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Graphene has been attracting wide attention owing to its superb electronic, thermal and mechanical properties. These properties allow great applications in the next generation of optoelectronics, where flexibility and stretchability are essential. In this context, the recent development of graphene growth/transfer and its applications in field-effect transistors are involved. In particular, we provide a detailed review on the state-of-the-art of graphene-based flexible and stretchable thin film transistors. We address the principles of fabricating high-speed graphene analog transistors and the key issues of producing an array of graphene-based transistors on flexible and stretchable substrates. It provides a platform for future work to focus on understanding and realizing high-performance graphene-based transistors.

1. Introduction

The outstanding physical and chemical properties of graphene, a single atomic layer of carbon atoms, have attracted significant attention. One of the most important advantages of graphene in the field of electronics is its superb charge carrier mobility. The mobility of ideal exfoliated graphene spans an extraordinarily large range, from 10 000–15 000 $cm^2\ V^{-1}\ s^{-1}$ on SiO_2 insulating substrates to 200 000 $cm^2\ V^{-1}\ s^{-1}$ in suspended structures,[1–5] suggesting that graphene may potentially outperform established inorganic materials in certain applications, such as high-frequency transistors. Although useful devices have been prepared based on exfoliated graphene,[6] the tiny size of exfoliated graphene films limits the practical utility of such graphene in electronic applications. Recent studies designed to address this issue have explored the preparation of large-area high-quality graphene *via* epitaxial growth[7,8] or chemical vapor deposition (CVD).[9,10] Many research groups have reported the fabrication of graphene-based transistors *via* the epitaxial growth of

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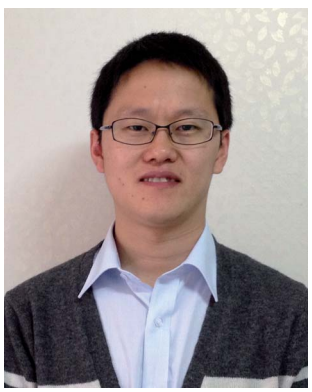

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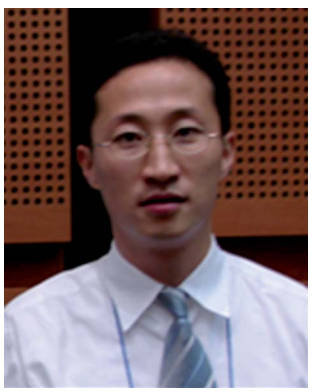

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graphene directly on rigid insulating silicon carbide (SiC) wafers. These transistors operate at high frequencies, up to 100 GHz.[11] Other researchers have synthesized graphene on Ni or Cu catalysts using CVD methods and have demonstrated the utility of device integration on a variety of substrates using transfer techniques. The CVD approach is attractive because it permits fabrication over large areas and expands the applicability of graphene to flexible or fully stretchable devices on thin plastic or elastomeric substrates.[12–14]

This article summarizes recent progress in graphene film preparation and discusses graphene film applications in the field of flexible and stretchable electronics, with particular focus on techniques for fabricating and integrating graphene into devices on compliant substrates. After discussing general approaches to the production and transfer of high-quality graphene films, we highlight the use of graphene in high-performance radio frequency transistors and flexible/stretchable electronic devices. Finally, we conclude with a brief perspective on the trends in the field and directions for future work.

2. Graphene synthesis and properties

2.1 Graphene synthesis and transfer

Since the preparation of single-layer graphene sheets in 2004 by Geim and Novoselov *et al. via* mechanical exfoliation of highly oriented pyrolytic graphite (HOPG),[6,15] a variety of processes have been developed for producing layered graphene. The famous Scotch tape method is representative of mechanical exfoliation approaches. In this method, a piece of Scotch tape is used to detach a thin layer from a graphite crystal. Repeated attachment and detachment of the tape then releases flakes of single-layer graphene onto a SiO_2 substrate, stabilized by van der Waals-mediated attraction between the graphene and the SiO_2 substrate. A single-layer graphene on a SiO_2/Si substrate can exhibit a 2.3% optical absorption over a broad spectral range (Fig. 1a).[16–18] This simple and effective approach has provided a valuable route to preparing single- and multiple-layered graphene and/or other two-dimensional atomic crystals, *e.g.* MoS_2 and hBN, on top of a variety of substrates. Mechanically exfoliated graphene yields high-quality structural integrity due to its low concentration of defects, which makes it well-suited for fundamental research; however, graphene produced by mechanical exfoliation is limited by its low production yield and reproducibility.

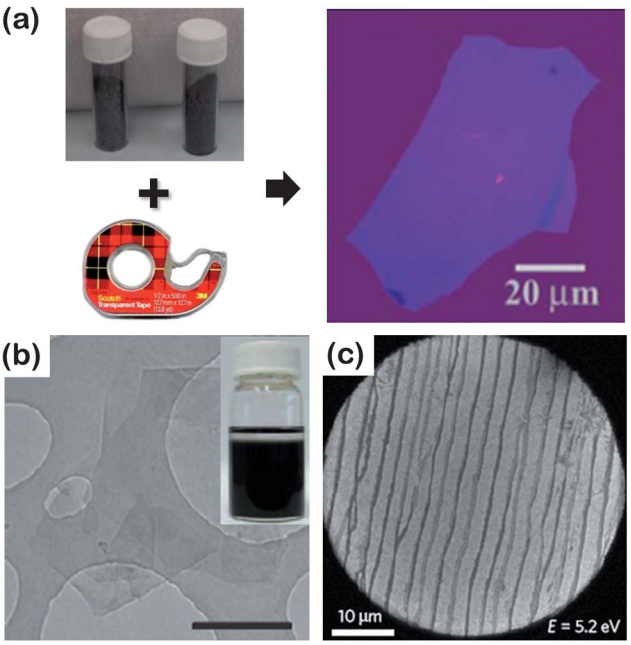

Fig. 1 (a) Schematic drawing showing the Scotch tape exfoliation method and a few layered graphene flakes on a SiO_2/Si substrate. (b) Bright-field TEM image of a few layered graphene sheets deposited from NMP (scale bar: 500 nm). (c) LEEM image of epitaxially grown graphene on 6H-SiC (0001). Adapted from ref. 6, ref. 7 and ref. 20 with permission.

Graphite exfoliation in liquids *via* covalent and noncovalent interactions provides an alternative method for preparing reproducible and scalable graphene films.[19–26] In the noncovalent interaction approach, strong interactions between the solvent and the graphite layers facilitate the exfoliation process. Several organic solvents with surface tensions that match that of graphene, 40 mJ m^{-2}, including *N*-methylpyrrolidone (NMP), *N*,*N*-dimethylacetamide (DMA), and dimethylformamide (DMF), have been found to effectively exfoliate graphite and produce graphene sheets.[19–23] Single- and few-layer graphene sheets can be obtained by this method (Fig. 1b). Vacuum filtration,[22] spray coating,[21] and Langmuir–Blodgett[23] techniques may be utilized to fabricate thin graphene films using liquid phase exfoliated graphene dispersions. The resulting graphene films yield low conductivities relative to pristine graphene films due to the large contact resistance between adjacent graphene sheets and the presence of solvent and surfactant residues. Covalent interaction exfoliation processes are aided by the chemical modification of graphite to produce water-dispersible graphite oxide (GO). After oxidation, GO is readily exfoliated due to strong interactions between the water and oxygen-containing functional groups, such as hydroxyl and epoxide groups, introduced to the sheets during the oxidation process.[24,25] The resulting GO suspension can be reduced to graphene by, for example, thermal or chemical reduction. Due to the low cost and massive scalability of GO-based graphene preparation methods, significant effort has been applied toward improving the film performance, such as repairing defects and chemical doping.[27–33]

Jong-Hyun Ahn

Jong-Hyun Ahn obtained his PhD from POSTECH, Republic of Korea in 2001. From 2004 to 2008, he was a research associate at the University of Illinois at Urbana-Champaign. In 2008, he joined Sungkyunkwan University, Republic of Korea, where he has been an associate professor and SKKU fellow since 2012. His research interests focus on inorganic nanomaterials, graphene and their application in flexible electronics.

The thermal decomposition of SiC can generate wafer-scale few-layered graphene films that are potentially interesting to the semiconductor industry.[7,8,11,34–39] Fig. 1c shows a low-energy electron microscopy (LEEM) image of graphene grown on a SiC substrate annealed under ultra-high vacuum (UHV).[7] Several challenges to this approach must be addressed, including control over the number of graphene layers and the size of the continuous graphene sheets. The number of graphene layers typically depends on the decomposition temperature. Optimized synthesis conditions yield millimeter-size few-layer graphene in conjunction with a SiC substrate coated onto a thin Ni film.[34] This technique produces high-quality uniform graphene on insulating substrates without the need for additional transfer processes. Ultra-high-speed graphene transistors with switching speeds of up to 100 GHz have been fabricated using this technique.[11] In addition, an effective transfer method of graphene films on SiC substrates to arbitrary substrates has been developed,[40,41] similar to single-walled carbon nanotubes (SWCNT).[42] Au (or Pd)/polyimide bilayers were deposited on graphene-grown SiC wafers, and the graphene layers were peeled off with the aid of a strong baked polyimide thin film support. The Au/polyimide/graphene layers were then transferred onto a desired substrate, and the Au–polyimide layers were removed by oxygen plasma reactive ion etching (RIE) and wet chemical etching.

Unlike thermal decomposition methods, which use high-cost SiC substrates, chemical vapor deposition (CVD) utilizes inexpensive and readily accessible Ni and Cu substrates.[9,10,12,43,44] With recent advances, CVD techniques yield the repeatable and reliable production of large-area, high-quality graphene films on Ni or Cu foils. The metal serves as both a catalyst and a substrate for growing graphene layers in the context of the CVD. The mechanism underlying the CVD growth of graphene on transition metal substrates, such as Ni and Cu, involves the diffusion of carbon into a thin metal film at a desired growth temperature, the subsequent precipitation of carbon out of the metal thin film due to reduced solubility upon cooling, followed by the formation of layered graphene on the metal surface. The thickness and crystalline ordering of the resultant graphene films depend on the concentration of the carbon source dissolved in the catalyst substrate and the cooling rate. Fig. 2a shows a confocal scanning Raman spectroscopy image of few-layer graphene grown on a Ni catalyst. The contrast variations in the image indicate graphene films of different thicknesses. Brighter areas correspond to thinner graphene and darker areas correspond to thicker layers, as indicated by the markers in the Raman spectra shown in Fig. 2c. The ratio of the G and 2D Raman band intensities (G/2D) provides an estimate for the numbers of graphene layers. The low intensity of

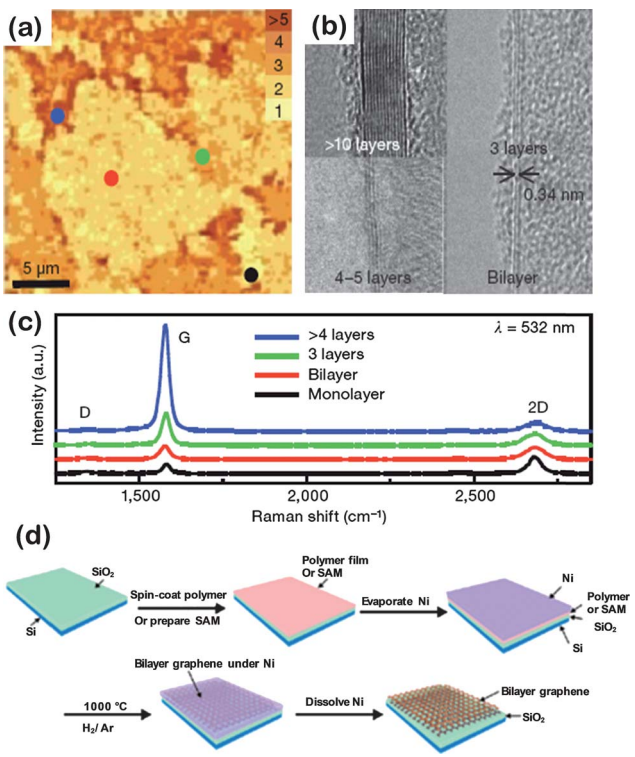

Fig. 2 (a) Confocal scanning Raman image of graphene synthesized on a Ni substrate by CVD. (b) Thickness and interlayer distance of the as-grown graphene film, estimated by HRTEM. (c) Raman spectra at each point in (a), indicating the number of layers present. (d) Synthetic protocol for preparing bilayer graphene on a SiO_2/Si substrate using a Ni thin film catalyst. Adapted from ref. 10 and ref. 46 with permission.

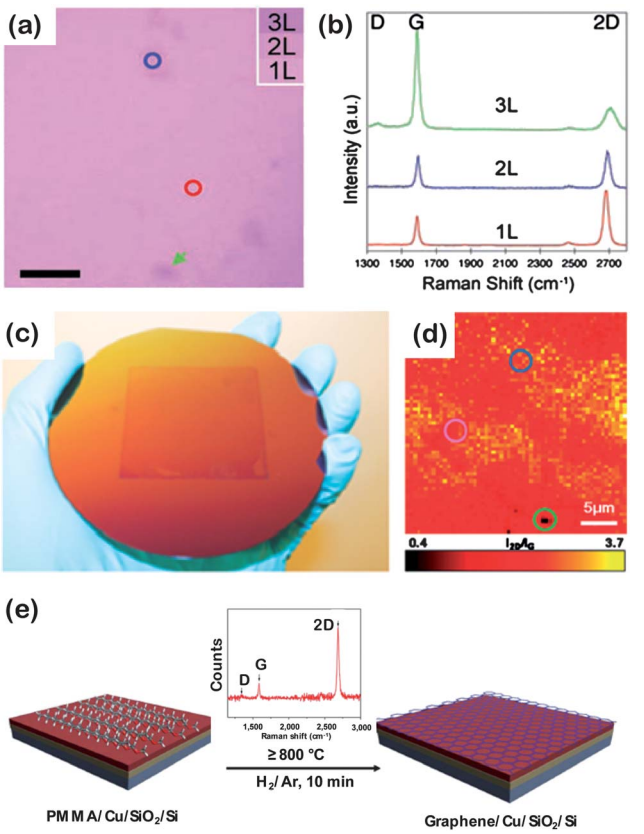

Fig. 3 (a) Optical microscopy image of a graphene film transferred onto a SiO_2/Si substrate; the colors indicate the number of layers. (b) Raman spectra for various numbers of graphene layers, collected at the positions indicated in (a). (c) Photograph of a 2 × 2 inch bilayer graphene film transferred onto a 4 inch SiO_2/Si substrate. (d) Two-dimensional color mappings of the I_{2D}/I_G ratio from the Raman spectra collected over a 30 × 30 μm area of CVD bilayer graphene. (e) Schematic illustration of the synthesis of monolayer graphene from a solid carbon source (such as PMMA) on a Cu substrate; the inset shows the corresponding Raman spectrum of the resultant graphene film. Adapted from ref. 9, ref. 47 and ref. 50 with permission.

the D peak in the Raman spectra indicates a low defect density in the resultant graphene film. The exact number of graphene layers can be determined by transmission electron microscopy (TEM), as shown in Fig. 2b. The relatively high solubility of carbon in Ni substrates favors the generation of multiple-layer graphene on Ni catalysts under standard conditions. Remarkably, recent developments in the uniform deposition of bilayer graphene using Ni thin film catalysts have provided access to transfer-free bilayer graphene on insulating substrates (Fig. 2d).[45,46]

The deposition of high-quality single-layer graphene on Cu foils over large areas by CVD processes has recently been achieved.[9] The CVD process for graphene growth on Cu substrates is a surface-mediated process that terminates once the Cu surface reaches full coverage with graphene. Surfaces with more than 95% monolayer graphene coverage have been demonstrated, as determined by optical microscopy and Raman spectroscopy, see Fig. 3a and b. Recently, the synthesis of uniform bilayer graphene films on wafer-size Cu substrates was explored (Fig. 3c). A bilayer coverage exceeding 99% was obtained, as confirmed using spatially resolved Raman spectroscopy (Fig. 3d).[47] Significant efforts have focused on the development of routes to improving the quality or accessibility of CVD-grown graphene, including the use of solid or liquid carbon sources instead of gaseous raw materials (Fig. 3e), two-step CVD deposition, or Cu substrate treatment.[9,43,48–52]

In order to investigate the optoelectronic properties and utilize graphene in various electronic applications, as-grown graphene films on Ni or Cu substrates must be transferred to target substrates. Efficient transfer techniques must minimize film damage and preserve the excellent properties of graphene. Several techniques have been developed for transferring large-area graphene films grown on Ni or Cu surfaces.[10,12,43,53–57] A current generally accepted transfer method uses polymethylmethacrylate (PMMA) or polydimethylsiloxane (PDMS) as a supporting layer. A graphene surface is coated with PMMA or PDMS, and the metal catalyst is then etched using an etchant. The polymer-supported graphene is then readily transferred onto a desired substrate, and the supporting layer is removed.[9,12,57] The successful transfer of large-scale graphene has been achieved using a roll-to-roll transfer method with a support layer comprising thermal release tape. As shown in the schematic diagram (Fig. 4a),[43] the process enables the production of large-area graphene layers (as large as 30 inches) with excellent optical (97.4% transmittance at 550 nm) and electrical (125 Ω per sq sheet resistance for a single layer) properties. Multiple-stacked graphene films may be obtained by repeating this process. Recently, a promising high-efficiency, recyclable, nondestructive electrochemical technique was applied toward the transfer of CVD-grown graphene films from a metal substrate (Fig. 4b).[53] The resultant graphene exhibited better electronic performances after several synthesis cycles on the reused Cu substrate. Another novel approach involving the use of a recycled metal catalyst was explored by taking advantage of the covalent bonds between specific polymers and the CVD-grown graphene (Fig. 4c).[56] These transfer methods provide several options for transferring CVD-grown graphene from a metal catalyst surface to a target substrate. Fig. 5 shows photographs of graphene layers transferred to a variety of substrates, including rigid, flexible, and stretchable substrates.[12,43]

2.2 Graphene: optical, mechanical, and electric properties

The extraordinary properties of graphene have fueled the rapid evolution of research in both fundamental and industrial contexts. A brief description of the properties of graphene will provide a basis for understanding the graphene applications. The

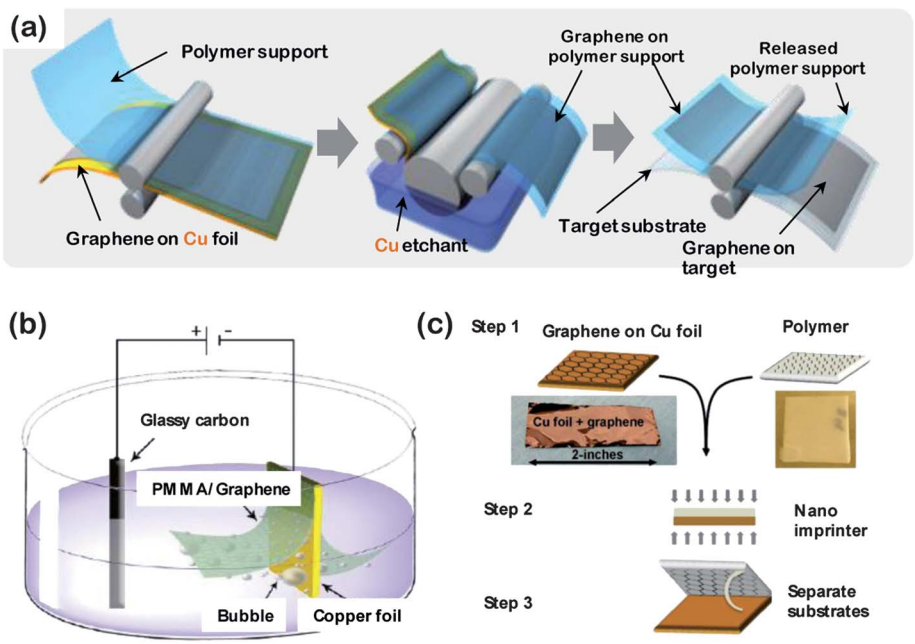

Fig. 4 (a) Roll-to-roll transfer of graphene grown on a Cu foil, using thermal release tape. (b) Schematic diagram of the electrochemical transfer of graphene from a metal substrate using an electrochemical cell. (c) Dry transfer process involving covalent bonding. Step 1: monolayer graphene was synthesized on a Cu foil; the polymer surface was treated to increase its reactivity. Step 2: both substrates were placed in a Nano Imprinter. Step 3: the substrates were separated and graphene was transferred onto the polymer. Adapted from ref. 43, ref. 53 and ref. 56 with permission.

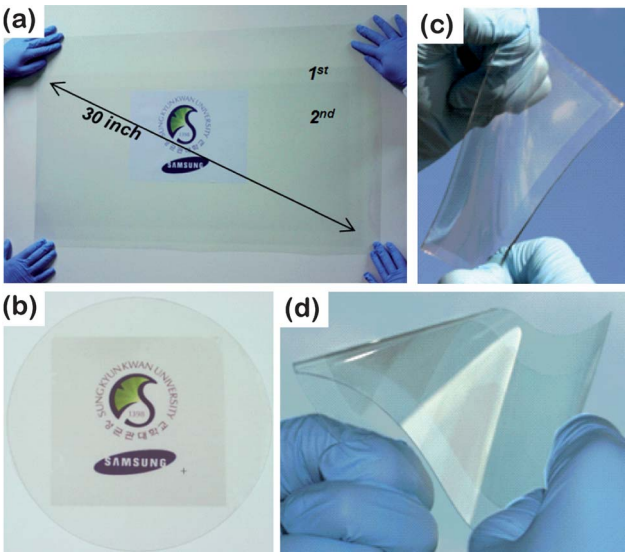

Fig. 5 The transfer of graphene onto a variety of substrates. (a) Roll-to-roll transfer of an ultra-large-area graphene film on a 35 inch PET substrate. Photographs of a graphene film transferred on a rigid transparent substrate (b), a stretchable PDMS substrate (c) and a flexible PET substrate (d). Adapted from ref. 12 and ref. 43 with permission.

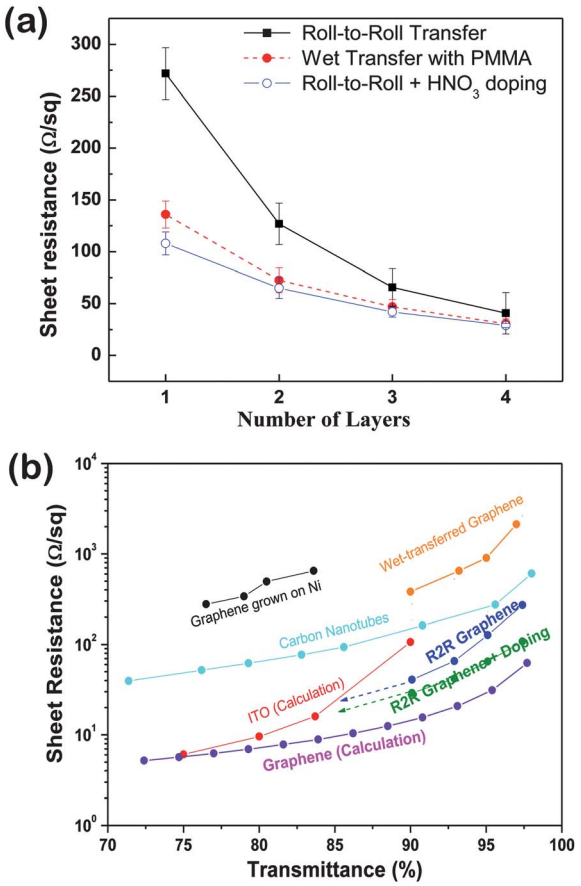

Fig. 6 (a) Sheet resistances of graphene films transferred by a roll-to-roll process, a combination of roll-to-roll and acid doping, or wet transfer using a PMMA supporting layer. (b) Comparison of the sheet resistance and transparency values, from the references listed. Adapted from ref. 43 with permission.

optical absorption of single-layer graphene is 2.3% over a broad spectral range.[16,43,58] The optical transparency of CVD-grown randomly stacked graphene sheets decreases in proportion to the number of graphene layers.[10,43] The sheet resistance of stacked graphene sheets, on the other hand, deceases dramatically with the number of stacked graphene layers, as shown in Fig. 6a,[43] because any defects introduced during the transfer process are compensated by the random stacking of the layers. The roll-to-roll transfer method produces large-area graphene films yielding sheet resistances of 30 Ω sq^{-1} and optical transmittances of 90% for four-layer stacked graphene after p-doping with nitric acid, comparable to the properties of indium tin oxide (ITO) transparent electrodes. Fig. 6b shows the sheet resistance and transparency values of ITO, carbon nanotubes, and CVD-grown graphene. The sheet resistance of doped roll-to-roll transferred graphene is much lower than that of other materials at the same transparency.[43] The sheet resistance and transparency alone may permit multi-stacked, doped CVD-grown graphene on Cu catalysts to replace ITO. It is worth noting that the optimal conductivities of graphene obtained experimentally are far below the ideal theoretically predicted conductivity. Improvements in the graphene quality and the proficiency of the transfer technique may make transparent conductive graphene films more competitive for use in modern devices.

Graphene displays outstanding mechanical flexibility upon bending and stretching. Fig. 7a compares the performances of a single-layer graphene and common ITO during bending.[43] ITO electrodes could not survive under strains exceeding 3%; however, the resistance values of graphene films did not change significantly, even under strains exceeding 6%. The transfer of a graphene sheet onto a stretchable substrate, such as PDMS, permitted evaluation of the resistance during stretching processes. Fig. 7b presents the resistance changes of a graphene film on PDMS, transferred from a CVD-grown graphene layer on a Ni substrate, upon perpendicular or parallel stretching.[10] The resistance values of graphene films on PDMS substrates were fully recovered after up to 6% stretching. Transfer of a graphene film to an isotropically pre-stretched PDMS substrate and subsequent resistance measurements demonstrated that both the longitudinal and transverse resistance were stable up to strain levels of 11%. The unique mechanical characteristics of graphene are desirable for the fabrication of next-generation flexible stretchable electronics.

In addition to the sheet resistance, a common method for characterizing the electrical properties of graphene sheets is to measure the carrier mobility. The mobility of mechanically exfoliated, suspended single-layer graphene on a Si/SiO_2 substrate exceeded 200 000 cm^2 V^{-1} s^{-1} at a carrier density of 2×10^{11} cm^{-2}. The peak mobility after current annealing could reach 230 000 cm^2 V^{-1} s^{-1}, as shown in Fig. 8a,[1] much higher than the peak mobilities of typical semiconductors. Although suspended graphene exhibits a super-high mobility, this architecture cannot be applicable in the real graphene devices. The fabrication of high-speed graphene devices requires consideration of the effects of the underlying substrate on electronic transport. Unlike suspended graphene,[1–3] the electronic transport properties of graphene on SiO_2 substrates are moderately affected by the substrate properties, including ripples, surface charge traps, or interfacial

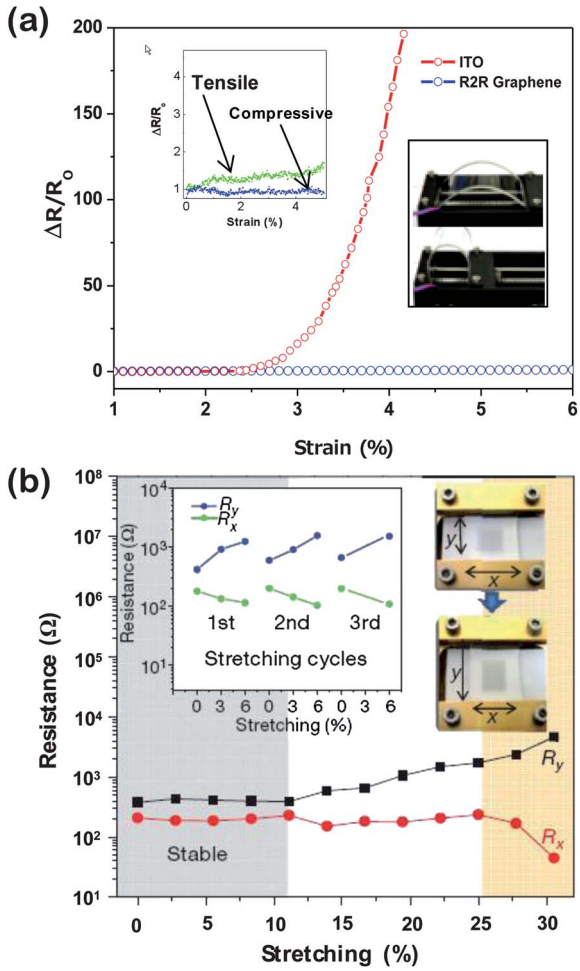

Fig. 7 Mechanical flexibility (a) and stretchability (b) of graphene. (a) Resistance properties of CVD-grown graphene transferred onto a PET substrate in comparison with ITO–PET electrodes under tensile strain. The inset of (a) shows the resistance as a function of the compressive and tensile strain applied to the upper and lower graphene–PET layers, respectively. (b) Resistance of a graphene film transferred onto a PDMS substrate isotropically stretched by 12%. The left inset shows the results of the graphene film transferred to an unstretched PDMS. The right inset shows the movement of the holding stages and the consequent changes in the graphene shape. Adapted from ref. 10 and ref. 43 with permission.

phonons.[4,5,59,60] Large-area graphene, synthesized by CVD and transferred onto SiO_2 substrates, normally yields a carrier mobility on the order of 10^3 cm^2 V^{-1} s^{-1}. The reasons underlying the reduced mobility have not been elucidated, but several factors, such as grain boundaries and doping effects, cannot be ignored.[61–63] Hexagonal boron nitride (hBN) may be an optimal substrate because it presents an atomically smooth surface, includes relatively few charge impurities, and yields high surface phonon frequencies. Fig. 8b shows the representative conductivity curves obtained from multilayer graphene samples transferred to hBN substrates.[64,65] The mobility of graphene on hBN is several factors higher than that of graphene on a SiO_2 substrate. With the recent development of large-area high-quality hBN growth by CVD,[65–70] the preparation of graphene/hBN-based devices may become feasible. Such devices are particularly promising for their potential use in flexible and stretchable devices.

3. Application of graphene to high-performance transistors

3.1 Graphene-based RF devices

The development of graphene field-effect transistors (GFETs) immediately followed the first observation of field-effects in graphene in 2004. The zero band gap in graphene induces a high off-current and a low on/off ratio, on the order of 100 or lower, which is much lower than the required values of 10^3 to 10^6 for logic applications.[6,71] Several efforts have been applied to broaden the band gap of graphene using bilayer graphene, nanoribbons, doping, and strain;[72–75] however, the extraordinarily high mobility of graphene, currently regarded the highest mobility yet achieved, makes graphene an attractive material for high-frequency applications, such as radio-frequency switches. The cut-off frequency (f_T) is defined as the frequency at which the current gain of a device becomes 1 and indicates the maximum frequency at which signals can be propagated in the transistor.[76,77] The f_T is determined by the transconductance (g_m) and capacitance (C) of the device, as expressed in the following equation.

$$f_T = \frac{g_m}{2\pi C}$$

A high cut-off frequency value can be achieved by increasing the transconductance and reducing the capacitance. The first graphene-based GHz radio frequency transistor was fabricated using exfoliated graphene in 2008, yielding a cut-off frequency of 14.7 GHz.[78] Graphene was exfoliated onto a Si substrate coated with a 300 nm thick layer of thermally grown SiO_2. Source and drain electrodes were prepared using electron-beam lithography, followed by a Cr/Au deposition. A HfO_2 thin film top-gate dielectric layer (30 nm in thickness) was then directly deposited by atomic layer deposition (ALD), followed by patterning of the Cr/Au gate electrodes. The fabrication step that presents the greatest difficulty in this process is the deposition of a uniform thin dielectric layer of a high-k material on top of the graphene layer. Graphene is inert and hydrophobic, and the interfacial strength between graphene and common polar insulators (such as HfO_2 and Al_2O_3) is poor. Several approaches to addressing this issue have been suggested, including using a third material or chemical functionalization to modify the interfacial properties. A fast GFET was realized using a functionalized buffer layer. Fig. 9a and b show the optical image and the architecture of a top-gate GFET operating with a cut-off frequency of 26 GHz. Exfoliated single-layer graphene was used as the active channel. Source–drain electrodes were patterned using electron-beam lithography. A functionalized layer of NO_2–TMA (trimethylaluminum) was deposited, followed by the preparation of a 12 nm thick Al_2O_3 gate insulator layer by ALD. Pd/Au (10/50 nm) layers were thermally deposited as gate electrodes. The value of f_T was found to be proportional to $1/L_G^2$ (where L_G is the gate length). Qualitatively, this relation indicates that the short gate length increases the drift velocity of the charge carriers by increasing the electric field and reduces the transit time across the transistor. By reducing the gate length from 500 to 150 nm, the maximum f_T was increased from 3 to 26 GHz (Fig. 9c).[79]

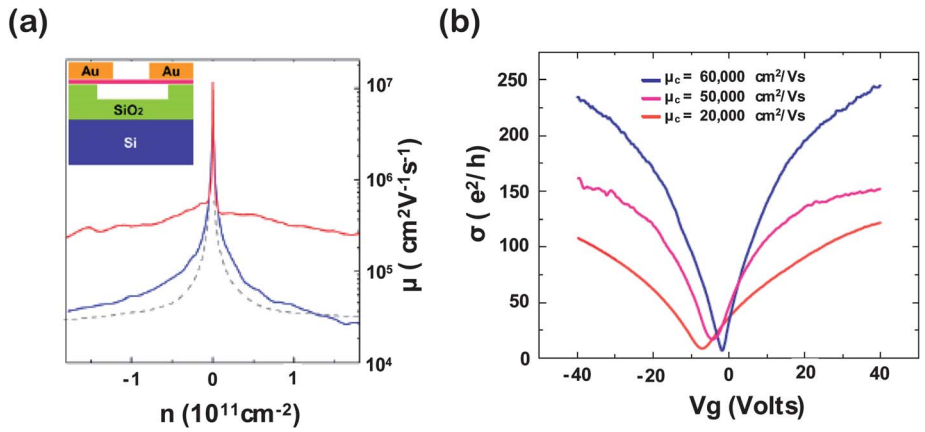

Fig. 8 (a) Carrier mobility as a function of the carrier density (n) for devices before (blue) and after (red) current annealing; data from a traditional high-mobility device on a substrate (gray dotted line) are shown for comparison. The inset shows a side view of the device schematic. (b) Representative conductivity curves measured for three different multilayer graphene films transferred onto hBN substrates. Adapted from ref. 1 and ref. 64 with permission.

For these GFETs, the estimated carrier mobility was 400 cm^2 V^{-1} s^{-1}. High-quality graphene, grown epitaxially on a 2 inch SiC substrate, was used to fabricate radio frequency GFETs with an effective mobility of 1000–1500 cm^2 V^{-1} s^{-1}. Polyhydroxystyrene was introduced as an interfacial polymer layer prior to the deposition of a 10 nm thick HfO_2 dielectric layer. The resultant GFETs presented a 100 GHz cut-off frequency with a gate length of 240 nm (Fig. 9d and e).[11]

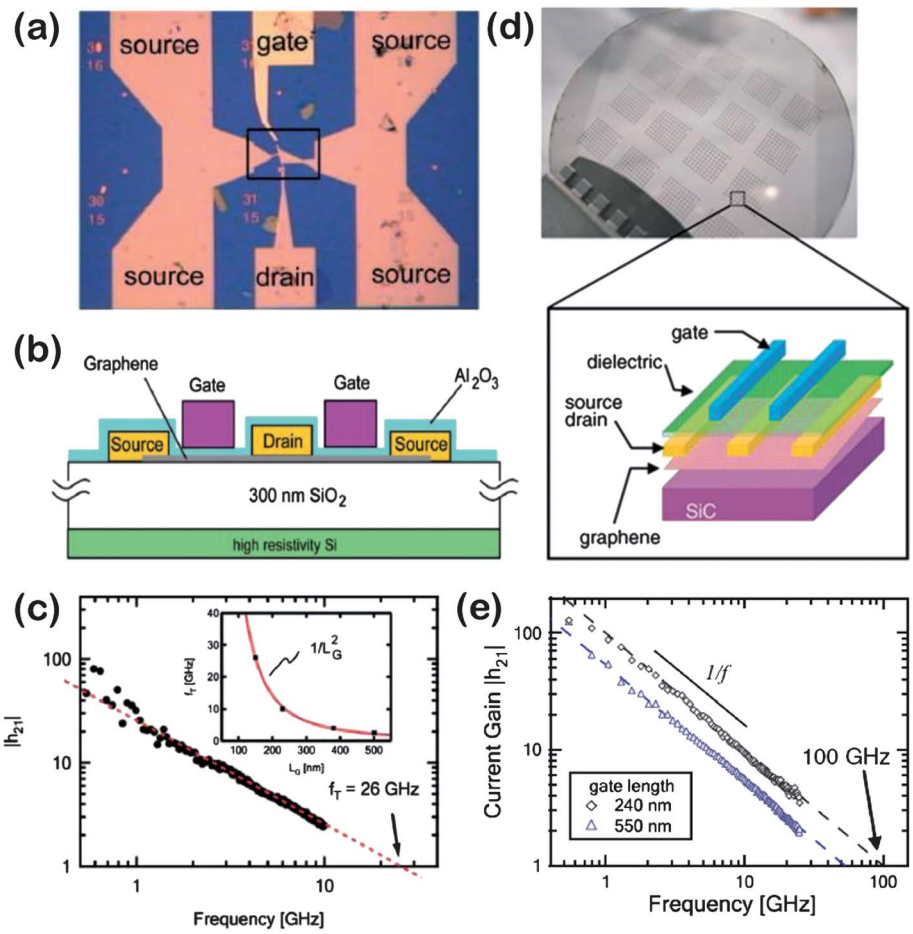

Fig. 9 (a) Optical image of the device layout of GFET having a cut-off frequency in the GHz range. (b) Schematic diagram of the GFET on a Si/SiO_2 substrate (c) with a cut-off frequency of 26 GHz. (d) Optical image of GFETs fabricated on a 2-inch graphene wafer and a schematic cross-sectional view of a top-gate GFET. (e) Small-signal current gain $|h_{21}|$ of the FETs shown in (d) as a function of frequency f for a 240 nm gate (◇) and a 550 nm gate (△) GFET at $V_D = 2.5$ V. The cut-off frequencies, f_T, were 53 and 100 GHz for the 550 nm and 240 nm gate length devices, respectively. Adapted from ref. 11 and ref. 79 with permission.

Following these results, a promising approach to fabricating high-speed GFETs was developed using a self-aligned Co_2Si/Al_2O_3 core–shell nanowire as the gate electrode/dielectric (Fig. 10a and b).[80] Source–drain electrodes were patterned using a self-alignment process, and the channel length was defined by the diameter of the nanowire. The device configuration minimized the degradation of the carrier mobility of graphene, and the resulting cut-off frequency was 100–300 GHz with gate lengths of 200 nm. Thus far, 300 GHz is the highest cut-off frequency yet achieved for graphene-based FETs. The RF performances of graphene-based FETs are much lower than the values predicted based on the intrinsic saturation velocity of graphene channels.[81] The carrier mobility and, thus, the cut-off frequency can be increased by addressing several aspects, including minimizing the defects and impurities in graphene and reducing the contact resistance.[82,83] A wafer-scale graphene circuit was recently prepared using innovative integration processes and circuit designs (Fig. 10c and d).[84] All GFETs and inductors were monolithically integrated onto a SiC wafer using arrays of graphene analog circuits, and the integrated circuit operated as a broadband radio frequency mixer at frequencies up to 10 GHz.

As discussed, most approaches to graphene applications in RF devices have focused on the use of rigid substrates, for example, a SiC wafer. The high mobility and flexibility of graphene has been exploited in the preparation of flexible graphene-based RF devices, as shown in Fig. 11. Top-gate solution-prepared GFETs were fabricated on polyimide foils with a source–drain distance of 260 nm, a gate length of 170 nm, and a gate width of 40 μm (Fig. 11a).[85] The resulting flexible graphene transistors exhibited

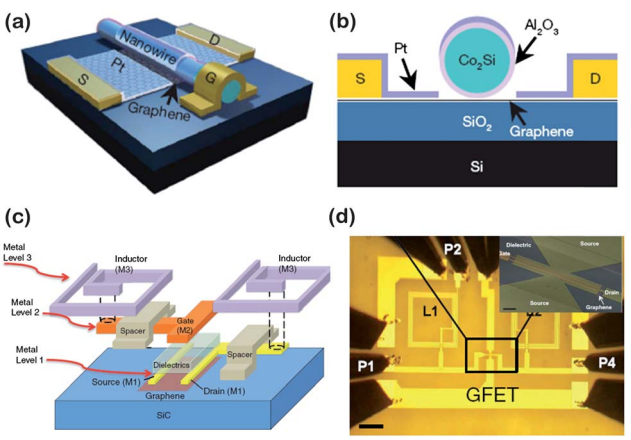

Fig. 10 Three-dimensional schematic illustration (a) and cross-sectional view (b) of a high-speed GFET with a Co_2Si/Al_2O_3 core–shell nanowire self-aligned top gate. In this device, the Co_2Si/Al_2O_3 core–shell nanowire defined the channel length, the 5 nm Al_2O_3 shell functioned as the gate dielectric, the metallic Co_2Si core functioned as the self-integrated local gate, and the self-aligned platinum thin film pads functioned as source and drain electrodes. (c) Schematic illustration of a graphene mixer circuit. The critical design aspects include a top-gate graphene transistor and two inductors connected to the gate and drain of the GFET. The three distinct metal layers of the graphene integrated circuit are indicated as M1, M2, and M3. A layer of 120 nm thick SiO_2 was used as the isolation spacer to electrically separate the inductors (M3) from the underlying interconnects (M1 and M2). (d) Optical image of a completed graphene mixer. Adapted from ref. 80 and ref. 84 with permission.

a current gain cut-off frequency (extrinsic f_T) of 2.2 GHz and a power gain cut-off frequency (f_m) of 550 MHz. Bending tests of the flexible RF devices revealed remarkable mechanical stability. These successful demonstrations highlight the practical applications of GFETs with complex functionalities.

3.2 Graphene-based flexible and stretchable transistors

In addition to flexible radio frequency transistors, the advantages of graphene's outstanding mechanical properties have found use in other flexible, stretchable electronics. Since the removal of the bottleneck in the synthesis and transfer of large-area, high-quality graphene, CVD-grown graphene films have shown promise for the fabrication of large-array flexible, stretchable transistors. Here, we describe recent advances in the preparation of flexible, stretchable transistors based on CVD-grown graphene as channels and/or electrodes.

An array of flexible field-effect transistors was fabricated on a flexible PET substrate using CVD-grown graphene source–drain electrodes and a single-walled carbon nanotube (SWNT) semiconducting channel,[86] as shown in Fig. 12a. This device presented a mobility of 2 $cm^2 V^{-1} s^{-1}$, an on/off ratio of 100, and robust mechanical bendability with small variations in the carrier mobility under strains of up to 2.2% (Fig. 12b). The integration of graphene and carbon nanotubes yielded devices with a high optical transparency. The transmittance values through the channel and source–drain regions, excluding the bare PET substrate, were 91% and 81% at 550 nm, respectively. One of the merits of graphene electrodes in CNT transistors is the negligible contact resistance, which is an important factor that affects the carrier mobility. Organic field-effect transistors with graphene electrodes exhibit low contact resistances compared with metal electrodes.[87–89] The contact resistance between an organic active layer and an electrode in a field-effect transistor can be estimated using the transfer line method (TLM).[90–92] High-performance organic FETs composed of a PEDOT:PSS gate electrode, a cross-linked polyvinylphenol (PVP) dielectric layer, a pentacene active channel, and graphene source–drain electrodes were recently prepared. The device architecture and performance are presented in Fig. 12c and d.[87] A device with graphene electrodes exhibited a carrier mobility of 0.54 ± 0.04 $cm^2 V^{-1} s^{-1}$ and an on/off ratio of 10^7, much higher than the values for devices with Au electrodes (0.02 $cm^2 V^{-1} s^{-1}$). The mobility difference between the two materials was attributed to the low contact resistance between the pentacene and graphene electrodes (two orders of magnitude lower than the contact resistance between pentacene and Au electrodes). Devices fabricated on a flexible PET substrate showed an average carrier mobility of 0.12 $cm^2 V^{-1} s^{-1}$.

Typical high-k gate dielectric insulators, such as Al_2O_3 and HfO_2, are not suitable for use in GFETs fabricated on flexible plastic substrates because they require a high growth temperature. High-capacitance gate dielectric materials that display good interfacial properties with graphene and can be processed at low temperatures are required. Solution-processable ion gel gate dielectrics were found to meet these requirements very well. Ion gels can be prepared by the gelation of a triblock copolymer, poly(styrene-methyl methacrylate-styrene) (PS-PMMA-PS) in an ionic liquid, 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM] [TFSI]) at room

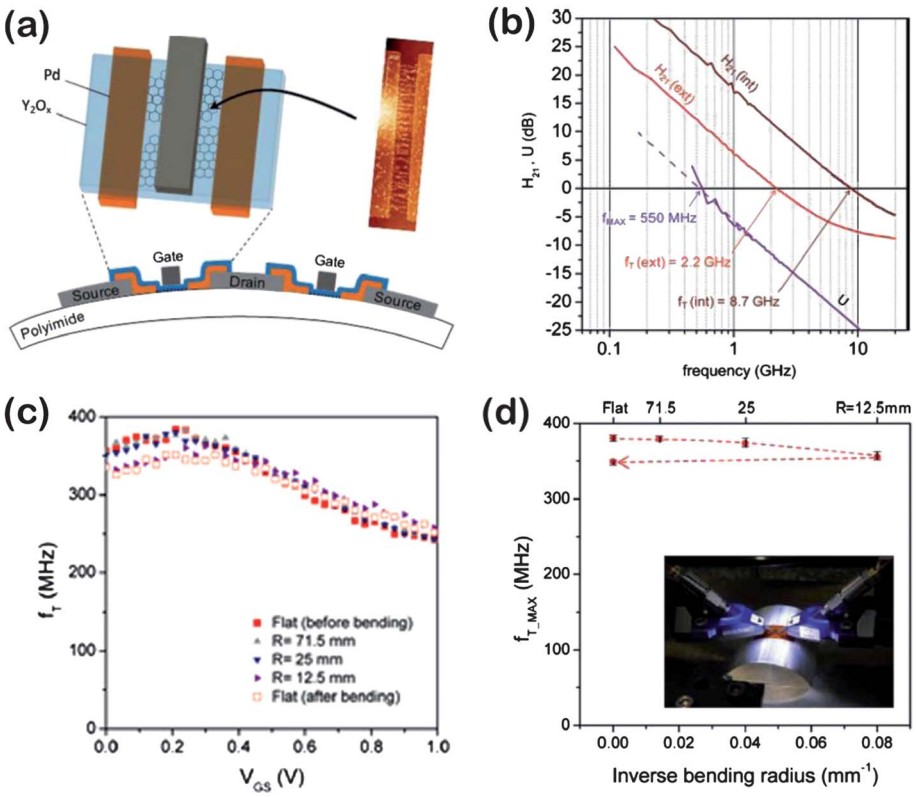

Fig. 11 (a) Schematic cross-sectional and top views of the top-gate GFET in a ground–signal–ground (GSG) configuration and an AFM image of the graphene flakes deposited by dielectrophoresis (DEP), acquired before deposition of the S/D and top gate electrodes. (b) The current gain (H_{21}) and power gain (U) as a function of frequency for the same device after current annealing. H_{21}(ext) is the as-measured (extrinsic) value, H_{21}(int) is the post de-embedded (intrinsic) value. (c) As-measured (extrinsic) current gain cut-off frequency as a function of the gate bias for samples in a flat configuration (before and after bending) or under bending at each of three angles. (d) The maximum extrinsic f_T extracted from figure (c), and a photograph of the test device under a bending angle of 25 mm. Adapted from ref. 85 with permission.

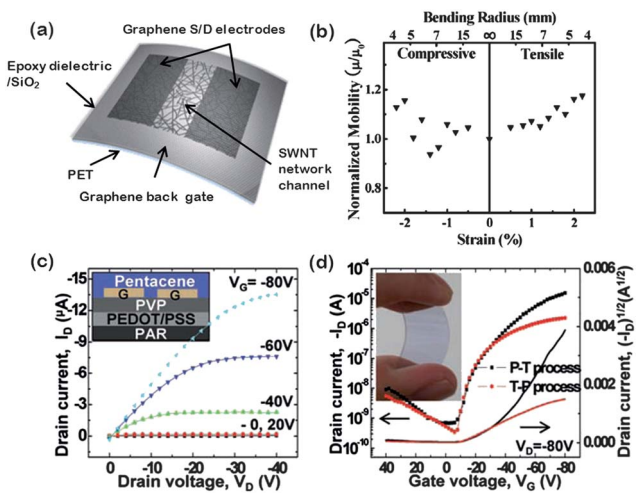

Fig. 12 A flexible transparent thin film transistor (TTFT) (a and b) and a flexible organic FET (c and d). (a) Schematic three-dimensional structure of a TTFT on a plastic substrate. (b) The normalized effective device mobility μ/μ_o of the TTFT as a function of the bending radius. Output characteristics (c) and transfer characteristics (d) of flexible organic FETs with graphene electrodes. The inset of (c) shows a schematic diagram of the cross-section of an FET. The inset of (d) shows a photograph of pentacene FETs showing the flexibility and transparency. Adapted from ref. 86 and ref. 87 with permission.

temperature. Ion gel films are readily formed by casting a solution containing [EMIM][TFSI] and PS-PMMA-PS directly onto a flat substrate and subsequently removing the solvent.[93–95] The capacitance of an ion gel film is 5.17 μF cm^{-2}, much higher than that of the commonly used 300 nm thick SiO_2 dielectric films. The high capacitance was attributed to the formation of thin electric double layers at the graphene–ion gel and ion gel–gate electrode interfaces under an electric field. Fig. 13a presents the scheme by which flexible GFET arrays were fabricated on plastic PET substrates.[13] Cr/Au was deposited by conventional photolithography onto the PET substrate to form source–drain electrodes. CVD-grown monolayer graphene was then transferred and patterned to build a channel. The ion gel solution was then drop-cast and the solvent was removed to form an ion gel dielectric layer. An Au top gate electrode was then prepared by thermal evaporation of Au through a shadow mask. A photograph of flexible GFET arrays and an optical image of the single devices are presented in Fig. 13b. The flexible GFETs showed excellent electrical performances at low voltages below 3 V with hole and electron mobilities of 203 ± 57 and 91 ± 50 cm^2 V^{-1} s^{-1}, respectively. It is worth noting that the low operating voltage is one of the great advantages of ion gel-gated GFETs. A symmetric bending test was performed to measure the mechanical flexibility of the ion gel-gated GFET arrays. Only small variations in the carrier mobility of less than 20% were observed

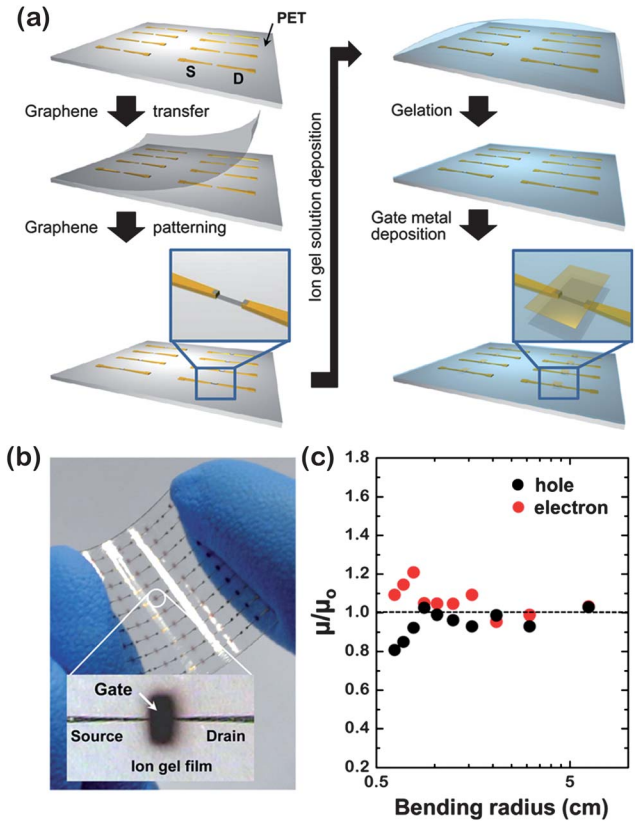

Fig. 13 (a) Schematic diagram showing the fabrication of an ion gel-gated graphene transistor array on a plastic substrate. (b) Optical image of an array of devices on a plastic substrate; the inset shows the structures of the single devices. (c) Normalized effective mobility (μ/μ_o) as a function of the bending radius. Adapted from ref. 13 with permission.

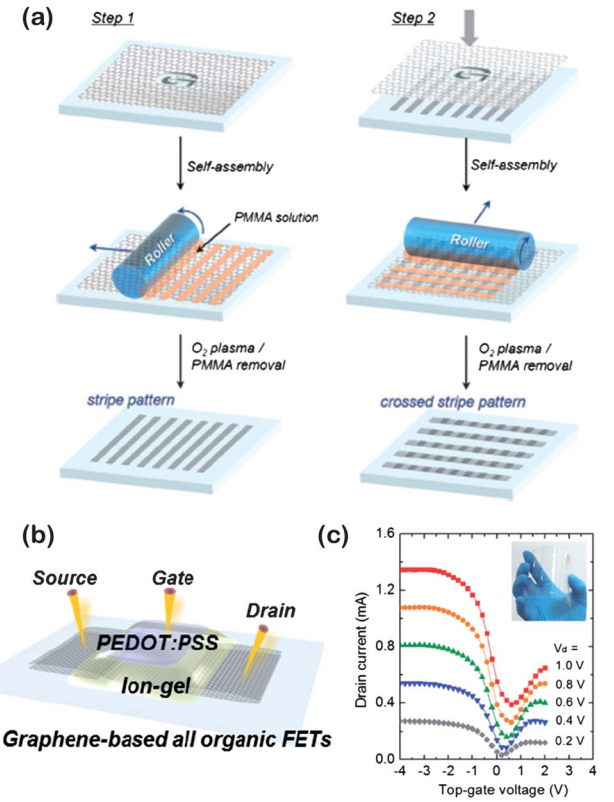

Fig. 14 (a) Schematic illustration of the graphene patterned using the EISA method. (b) Schematic three-dimensional structure of the single GFET devices. (c) Transfer characteristic of the GFETs as a function of V_D; the inset shows a photograph of the as-fabricated device arrays on a flexible transparent substrate. Adapted from ref. 96 with permission.

as the bending radius was decreased from 6 to 0.6 cm, as shown in Fig. 13c.

A delicate route to the fabrication of scalable graphene-based all-organic FETs was recently accomplished. The FET consisted of a PEDOT:PSS gate electrode, an ion gel gate insulator, a single-layer graphene active channel, and double-layer graphene source–drain electrodes.[96] The evaporation-induced self-assembly (EISA) technique produced highly ordered graphene patterns with crossed stripes of single- and double-layer graphene, as illustrated schematically in Fig. 14a. Fig. 14b shows the final architecture of each single device. Typical transfer characteristics of the resultant flexible ion gel-gated FETs with a single-layer graphene channel width and length of 16 μm are shown in Fig. 14c. All fabricated devices presented ambipolar behavior with a Dirac point and low voltage operation (below 4 V), along with hole and electron mobilities of 214 and 106 $cm^2\ V^{-1}\ s^{-1}$, respectively. The resultant GFET arrays on flexible PET substrates exhibited remarkable flexibility and transparency, as shown in the inset of Fig. 14c. The approach provides a viable route to the preparation of large-area graphene patterns without the need for conventional lithography.

All-graphene-based flexible field-effect transistors have been constructed using graphene electrodes, graphene channels, and graphene oxide gate dielectrics.[97] A GO layer fabricated using the Langmuir–Blodgett method exhibited good dielectric performances with a dielectric constant of 3.1 at 77 K, a low leakage current of 17 mA cm^{-1}, a breakdown bias of 1.5 MV cm^{-1}, and good mechanical flexibility. The bottom-gate all-graphene transistors were fabricated according to the following procedures. High-quality monolayer graphene was synthesized by CVD on Cu, then transferred onto the target substrate using methods described previously.[57] Lithography was used to build the graphene gate electrode, followed by the Langmuir–Blodgett deposition of a GO dielectric layer. Another monolayer of graphene was then transferred to the top of the GO and monolithically patterned to construct channel and source–drain electrodes without the use of traditional metal electrodes. Fig. 15a displays the device structures of all-graphene transistors. The fabricated FET arrays on flexible PET substrates showed good optical transparency, as shown in Fig. 15b and c. The combination of the excellent mechanical properties of graphene and GO and the tight bonding between each layer endowed the all-graphene transistors with outstanding mechanical flexibility. The devices operated stably under a tensile strain up to 3.5% (Fig. 15d). The all-graphene transistors constitute a significant step toward the use of graphene in future electronics.

In addition to optical transparency and flexibility, stretchability is an essential feature for next-generation modern electronics. The poor optical transparency and mechanical

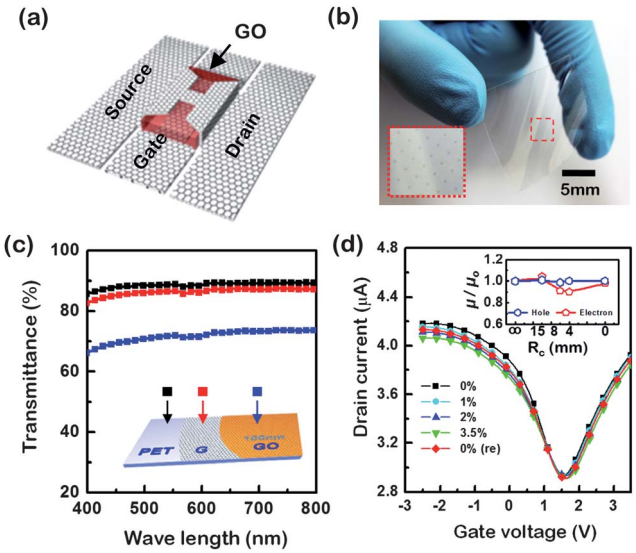

Fig. 15 (a) Schematic illustration of a bottom gated graphene–GO transistor. The graphene channel monolithically patterned with source–drain electrodes was positioned above the GO dielectric. (b) Optical image of the as-prepared all-graphene transistor arrays on a plastic substrate. (c) Optical transmittance as a function of wavelength for the PET substrate (black line), the monolayer graphene (red line), and the GO dielectric (blue line) of a device on a PET substrate. (d) Transfer curves measured as a function of the tensile strain (0–3.5%). The inset shows the effective mobility as a function of the bending radius.

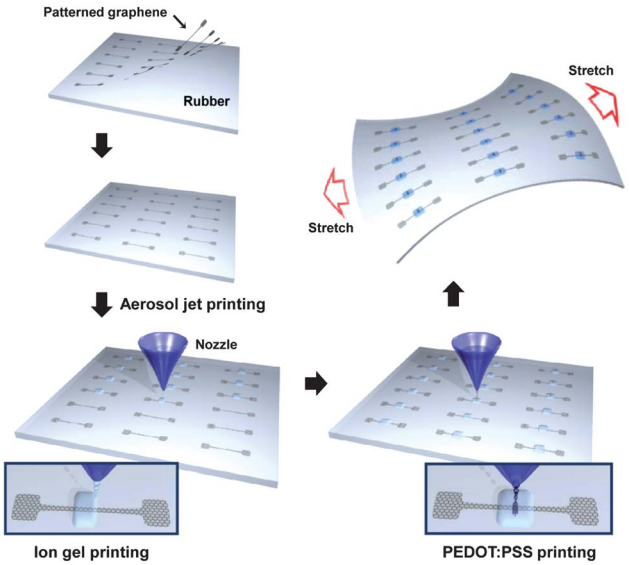

Fig. 16 Fabrication schematics of arrays of graphene FETs fabricated on a stretchable substrate. Adapted from ref. 14 with permission.

stretchability of conventional semiconducting materials have prevented the development of stretchable electronics. A variety of efforts have been attempted to overcome these obstacles by using specific structural designs[98–101] or stretchable interconnections.[102–111] These strategies offer device arrays or integrated circuits with high stretchability, even though individual components in a device are nearly unstretchable (the intrinsic stretchability is less than 1%). The outstanding mechanical properties of graphene provide significant potential for fabricating stretchable electronic devices with a high intrinsic stretchability. An amazing demonstration of field-effect transistors with a high intrinsic stretchability was realized by taking advantage of the unique mechanical properties of graphene and ion gel.[14]

Fig. 16 describes a fabrication scheme for preparing a stretchable GFET array on a rubber substrate. (1) High-quality monolayer graphene was synthesized on a Cu foil by CVD, then stacked *via* a layer-by-layer method using direct transfer.[112] (2) The active channel and source–drain electrodes were monolithically patterned using a graphene film. A photoresist was spin-coated on top of the graphene film as a supporting layer, followed by Cu etching. After etching, the patterned graphene was transferred onto the desired substrate, *e.g.*, PDMS. (3) A commercial aerosol jet printing technique was used to print an ion gel gate dielectric layer at room temperature. (4) In the last step, a conducting polymer ink containing PEDOT:PSS was printed over the channel as a gate electrode. The process produced GFET arrays on a variety of substrates, including flexible PET, stretchable PDMS, or rubber balloon. Fig. 17a and b show photographs of the stretchable FETs on balloons and PDMS substrates. The FET performance was measured over a strain range of 0–7% (Fig. 17c). Fig. 17d shows the typical transfer characteristics of a strained GFET on a PDMS substrate. The excellent stretchability of the graphene channel, electrodes, and ion gel dielectric resulted in the stable operation at strain levels up to 5%, even after 1000 cycles, with hole and electron mobilities of 1188 ± 136 and 422 ± 52 $cm^2 V^{-1} s^{-1}$, respectively. This technique opens a new route to fabricating high-performance stretchable electronics.

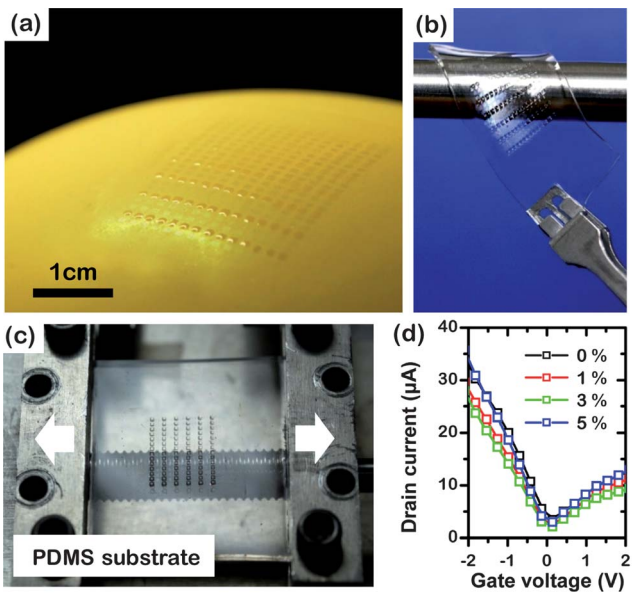

Fig. 17 Photographs of ion gel-gated graphene FETs on a balloon (a), or a PDMS substrate (b). (c) Home-built stretching machine for measuring the electrical performance of the ion gel-gated graphene FETs fabricated on stretchable PDMS substrates (with a thickness of 1.5 mm). (d) Typical transfer characteristics of the strained graphene FETs on PDMS. Adapted from ref. 14 with permission.

4. Conclusions and outlook

In this article, we have reviewed several recent works in the areas of high-performance graphene-based transistors for use in flexible and stretchable electronics. Approaches for producing high-quality graphene films, ranging from mechanical exfoliation to CVD methods, and a variety of integration methods for fabricating graphene devices on unusual substrates were discussed. The wide range of possibilities for applying graphene to the fabrication of electronics has inspired growing interest in the material. Although significant engineering challenges remain, including band gap broadening and improved reliability, graphene enables many novel approaches to the development of future electronic applications.

Acknowledgements

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