

Stretchable Graphene Transistors with Printed Dielectrics and Gate Electrodes

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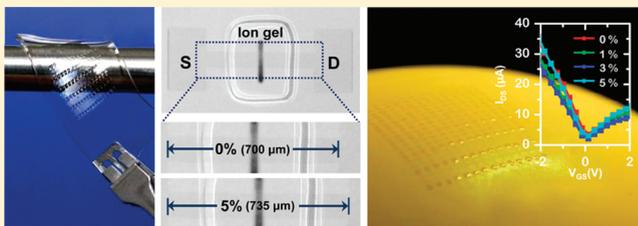
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S Supporting Information

ABSTRACT: With the emergence of human interface technology, the development of new applications based on stretchable electronics such as conformal biosensors and rollable displays are required. However, the difficulty in developing semiconducting materials with high stretchability required for such applications has restricted the range of applications of stretchable electronics. Here, we present stretchable, printable, and transparent transistors composed of monolithically patterned graphene films. This material offers excellent mechanical, electrical, and optical properties, capable of use as semiconducting channels as well as the source/drain electrodes. Such monolithic graphene transistors show hole and electron mobilities of 1188 ± 136 and 422 ± 52 $\text{cm}^2/(\text{V s})$, respectively, with stable operation at stretching up to 5% even after 1000 or more cycles.

KEYWORDS: Graphene transistor, stretchable devices, ion gel gate dielectric, printing process, low-voltage operation



Stretchable and transparent electronics can enable innovative classes of electronic applications for human interface technology.^{1,2} Such applications require electronic materials that can simultaneously exhibit excellent mechanical robustness, electronic functionality, and optical transmittance under a high strain.^{3–5} A variety of semiconductor materials have been explored for accomplishing this goal, ranging from small molecules and polymers to inorganic materials with various structural forms such as wires, ribbons, and platelets.^{6,7} One of the most significant hurdles to achieving transparent and stretchable devices using conventional semiconducting materials arise from their intrinsic limitations like poor mechanical stretchability and optical properties. As an alternative, graphene offers outstanding electrical, mechanical, and optical properties, with quantitative characteristics that, in many cases, outperform those of other known semiconducting materials.^{8–13} Many of these properties offer unique benefit in high-performance conformal, stretchable electronic devices.^{14–18}

Although several recent studies report the fabrication of flexible field-effect transistors (FETs) on plastic substrate using graphene thin films,^{19–21} significant challenges remain in the fabrication of graphene field effect transistors (FETs) that meet mechanical specification demands for stretchable electronics.

The main difficulties are (i) to develop low temperature, printing processes for materials that form the channel region, gate insulator, and electrodes on soft substrates with high thermal expansion coefficients²² and (ii) to overcome intrinsic limitations of mechanical properties associated with conventional materials and circuits through development of new materials or device architectures.²³

In this Letter, we present a promising route to the fabrication of an all-graphene-based FET array on a stretchable rubber substrate using a low-temperature printing process. First, all device components, including channel region and S/D electrodes, were transferred onto a substrate and then the gate insulator and gate electrode were printed in a manner that avoids the need for high-temperature processes. Second, all-graphene-based transistors, the source(S)/drain(D) electrodes, and semiconducting channels of which were monolithically patterned from graphene film, were fabricated on rubber substrates without the use of traditional metal electrodes. The resulting monolithic devices display

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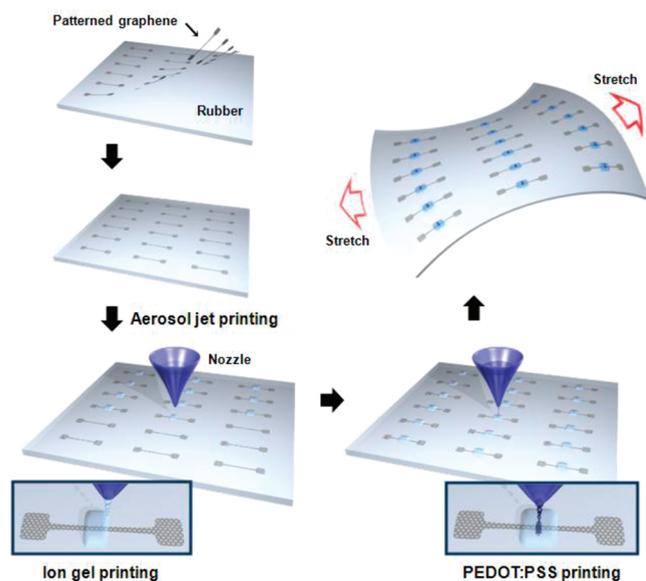


Figure 1. Schematic diagram of the fabrication procedure for arrays of graphene FETs on a stretchable substrate. Monolithically patterned graphene including source/drain electrodes and semiconducting channels were transferred on a rubber substrate with a supporting layer. After transfer, the supporting layer was removed with acetone. The ion gel gate dielectric and PEDOT:PSS gate electrodes were printed using commercial aerosol jet printing techniques.

several advantages, such as good mechanical stretchability, optical transmittance, and simple device design, as well as improved contact at the channel-to-S/D interface.

Figure 1 shows a schematic illustration of the steps involved in the fabrication of a graphene FET array on a rubber substrate. In the first step, high-quality monolayer graphene was synthesized on a large area Cu foil, as described previously¹⁷ and then the resulting material was stacked in a layer by layer fashion using direct transfer techniques (Figure S1, Supporting Information).¹⁸ The graphene patterns, including S/D electrodes and a semiconducting channel region, were defined by photolithography and oxygen plasma etching of graphene layers on Cu foil. The wide S/D region and the narrow long channel region were designed to optimize the effectiveness of the gate by adjusting its resistance. A photoresist (AZ 1512; commercial positive-type PR) supporting layer was spin-coated onto the graphene film on the Cu foil. The Cu metal catalyst was electrochemically etched using an aqueous 0.1 M ammonium persulfate solution. After etching, patterned graphene was transferred on rubber substrate as usual.¹⁵ For the low-temperature formation of the dielectric layer and gate electrode, a commercial aerosol jet printing technique was used (Figure S2, Supporting Information). The advantages of this jet printing method lie mainly in the high resolution (50 μm) and compatibility with various functional inks.^{22,24} Ion gel ink consisting of poly(styrene–methyl methacrylate–styrene) (PS-PMMA-PS) triblock copolymer and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) ionic liquid in ethyl acetate solvent (weight ratio of 0.1:0.9:9) was printed onto the patterned graphene. Upon solvent evaporation, PS-PMMA-PS triblock copolymer in the [EMIM][TFSI] ionic liquid formed a well-defined physical gel through noncovalent association of PS components that were insoluble in the ionic liquid. In the last step, a poly(3,4-ethylenedioxythiophene) oxidized with

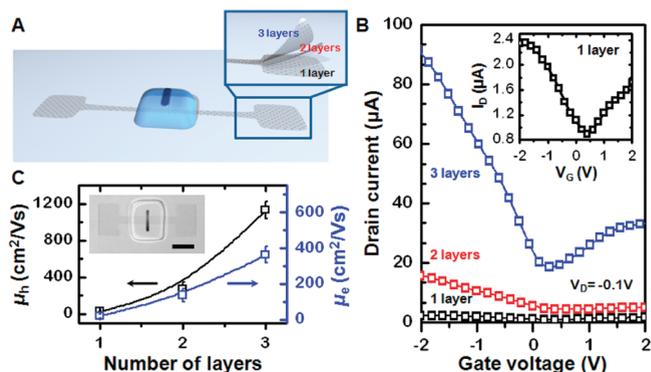


Figure 2. Schematic illustration and electrical characteristics of high-performance, transparent, stretchable graphene FETs on a PDMS rubber substrate. (A) Schematic diagrams of mono-, bi-, and tri-layer graphene FETs. (B) Transfer characteristics of graphene FETs as a function of the number of graphene layers. (C) Hole and electron mobilities of graphene FETs as a function of the number of graphene layers. The inset shows the microscopy image of tri-layer graphene FETs on PDMS (scale bar, 300 μm).

poly(4-styrenesulfonate) (PEDOT:PSS) gate electrode was printed over the channel. The conductivity of the printed PEDOT:PSS was measured to be 100 S/cm.

The outstanding mechanical properties of the graphene enabled device fabrication on rubber substrates, in ways that are not possible with conventional inorganic semiconducting materials. As a demonstration (Figure 2A), we fabricated high-performance, stretchable, and printable graphene FETs with high optical transmittance on poly(dimethylsiloxane) (PDMS) rubber (Figure S3:left, Supporting Information). Figure 2B shows the drain current (I_D) as a function of gate voltage (V_G) of the different layered graphene FETs. All the devices operate within a low voltage region (± 2 V) with a high on-current. The ultrahigh capacitance of the ion gel gate dielectric yielded this low-voltage, high-current operation. The specific capacitance of the ion gel was measured to be 5.17 $\mu\text{F}/\text{cm}^2$ at 10 Hz, much larger than typical values for 300 nm thick SiO_2 dielectrics (10.8 nF/cm^2). Clear ambipolar behavior was observed in the gate dependence of I_D , where a positive and negative V_G region represents electron and hole transport, respectively. The Dirac voltage which has the minimum conductance, for all the transfer curves was found to be at almost zero.²⁵

Unlike conventional transistors, the operation of ion gel gated transistors is based on the formation of a high capacitance electric double layer (EDL), at both the ion gel/semiconductor and ion gel/gate electrode interfaces under an electric field. For example, upon application of a negative gate bias, negative surface charges on the gate electrode attract positive [EMIM] ions and form an electric double layer at the ion gel/gate interface. At the same time, negative [TFSI] ions segregate to the ion gel/graphene interface. The two EDL are formed at the gate/ion gel and the ion gel/graphene interfaces with charge–neutral diffuse layer in between. Since the capacitance of this diffuse layer is negligible, the interfacial capacitance of ion gel can be then modeled as a serial combination of an electric double layer capacitance (C_{EDL}) and a quantum capacitance of the graphene (C_q).²⁶ As a consequence, the potential drop across the two capacitors is given by

$$|V_G - V_{G,\text{min}}| = \frac{h\nu_F\sqrt{\pi n}}{e} + \frac{ne}{C_{\text{EDL}}}$$

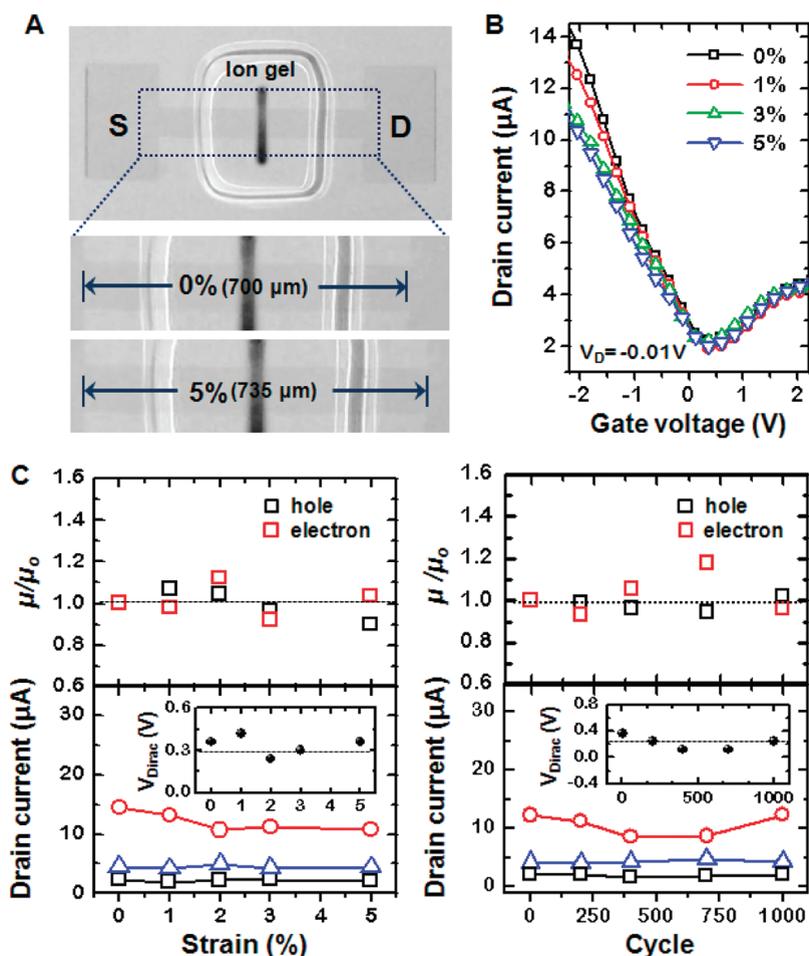


Figure 3. (A) Microscope images of tri-layer graphene FETs under substrate stretching up to 5% along the longitudinal direction of the channel. (B) Typical transfer characteristics of strained graphene FETs on PDMS. The device showed stable operation for stretching up to 5%, due to the excellent stretchability of the graphene and ion gel. (C) Normalized hole/electron mobilities, current levels (maximum hole (red circle)/electron (blue triangle), and the minimum current at the Dirac voltage (black square)) and Dirac voltage of graphene FETs as a function of the stretching level (left) and cycle during 3% device stretching and release (right).

where h is the reduced Planck's constant, v_F is Fermi velocity (1.1×10^6 m/s), e is the electron charge, and n is the charge density. On the basis of this equation, n was calculated by V_G , and the conductivity (σ) was plotted as function of n as shown in the right of Figure S3. From the slope of linear regimes in the σ vs n plot, the carrier mobility (μ) was calculated using $\mu = (d\sigma/dn)/e$. A quick formation of these two electric double layers is possible regardless of the area of overlap between the gate electrode and the active channel because it relies on the direct motion of highly mobile ions.²² As a consequence, unconventional device configurations in which the gate electrode does not fully cover the entire area of the graphene channel is possible (Figure 1).

First, monolayer graphene FETs were fabricated on PDMS substrate. The inset of Figure 2B shows the ambipolar transfer characteristics of the monolayer graphene FETs at $V_D = -0.1$ V. The average hole and electron mobilities were calculated as 26 and 20 $\text{cm}^2/(\text{V s})$, respectively. The poor carrier mobilities of the graphene FETs on PDMS substrate can be attributed to the both scattering from molecular species, such as moisture or other chemicals contained in the porous network structure of the PDMS²⁷ and exposing the graphene devices to contaminating species that can significantly reduce the transport properties.

To minimize the effects of PDMS-bound molecules, we fabricated bi- and tri-layer graphene-based FETs using multiple stacking method (Figure 2A). In these double- and tri-layer geometries, the bottom graphene layer provided sufficient screening of charged molecules on the substrates, acting as a barrier film; the top graphene layer was insensitive to the presence of moisture or other chemicals on the PDMS surface. In general, highly oriented multilayer graphene with an ABAB stacking sequence, as in graphite crystals, produces transistors with a lower on-current and on/off ratio due to interlayer coupling effects that become more prominent as the number of layers increases.²⁸ On the other hand, multilayer graphene films formed by transfer processes display weak interlayer coupling between layers due to the random orientations of the layer structures.¹⁷ As a result, device performance was dramatically improved compared with that achieved from monolayer graphene FETs (Figure 2B). Figure 2C shows hole and electron mobilities for different layered graphene FETs. The hole and electron mobilities increases with the number of graphene layers. The tri-layer graphene FETs yielded a hole mobility of $1131 \pm 96 \text{ cm}^2/(\text{V s})$ and an electron mobility of $362 \pm 45 \text{ cm}^2/(\text{V s})$, an order of magnitude greater than the corresponding values of the monolayer graphene FET.

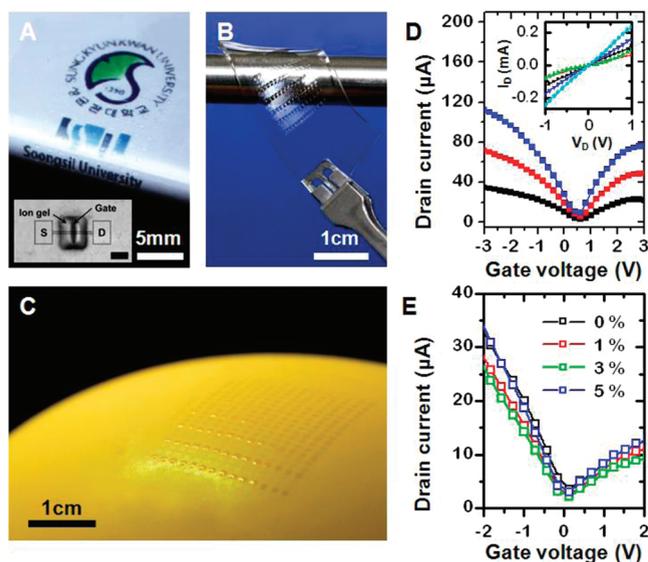


Figure 4. (A–C) Various images of the ion gel-gated graphene FETs on different substrate (polyethylene terephthalate (PET), PDMS and balloon). The inset shows the microscopy image of monolayer graphene FETs on PET (scale bar, 300 μm). (D) The transfer characteristics at three different V_D (–0.1 V (black), –0.2 V (red), –0.3 V (blue)) of monolayer graphene FETs fabricated on PET (channel widths of 20 μm and lengths of 500 μm). The hole and electron mobilities were 958 ± 237 and 512 ± 165 $\text{cm}^2/(\text{V s})$, respectively. Inset shows output characteristics of graphene FETs. In output curve, the gate voltage was varied between +2 V and –2 V in steps of –1 V. (E) Transfer characteristics of the tri-layer graphene FETs fabricated on a rubber balloon subjected to at most 5% strain ($V_D = -0.1$ V). The hole and electron mobilities were 435 ± 67 and 211 ± 38 $\text{cm}^2/(\text{V s})$, respectively, at 0% strain.

Uniaxial tunable tensile strain was applied to tri-layer graphene FETs with ion gel gate dielectrics by stretching the PDMS along the longitudinal direction of the channel. The device array was placed in a home-built uniaxial stretcher, with one side of the substrate fixed and the other side pulled to stretch the device (Figure S4, Supporting Information).

Figure 3A shows optical microscopy images of a graphene FETs at a device substrate stretching of 5%. FET performance was measured under 0–7% strain (Figure 3B and Figure S5, Supporting Information). The device exhibited stable operation at a strain of up to 5% due to the excellent stretchability of the graphene and ion gel. The hole and electron mobilities were calculated as 1188 ± 136 and 422 ± 52 $\text{cm}^2/(\text{V s})$, respectively, at 0% strain. The extensions of less than 5% yielded hole and electron mobility changes of at most 15%. Fatigue tests were performed on the graphene transistors. The electrical properties were invariant even after 1000 cycles of 3% stretching along the longitudinal direction (right frame of Figure 3C). The maximum hole and electron currents and the minimum current at the Dirac voltage were independent of stretching and fatigue (Figure 3C). The Dirac voltage did not shift significantly as shown in the inset of Figure 3C. However, degradation of device characteristics and broadening of the normalized mobility distribution were observed at large applied strains (above 5%), due at least partly to microcracks initiated by grain boundaries and/or by other defects in the graphene films (Figures S5 and S6, Supporting Information).²⁹

The good mechanical characteristics of graphene films enable integration onto highly compliant substrates, such as an ultrathin

plastic and a rubber material that are incompatible with conventional inorganic material-based electronics. As demonstrations, we fabricated graphene FETs on foldable plastic foil (Figure 4A, D), and freely deformable substrates such as rubber sheets and balloons (Figure 4B,C). Figure 4E shows the change in electrical properties of the graphene FETs during uniaxial stretching during inflation of the balloon. Graphene FETs on the balloon display excellent electrical properties without significant change during stretching. These results suggest that the graphene-based FETs can provide stable and robust operation during large-scale uniaxial and biaxial strain without any including special device designs, such as wavy or buckled configurations.

In summary, stretchable, transparent, monolithic graphene-based devices were realized by utilizing chemical vapor deposition grown graphene for both the semiconducting channel and the source/drain electrodes via low temperature printing procedures. This type of fabrication, without high temperature and vacuum processes, combined with intrinsically stretchable graphene films provides a promising route to creating electrical, optical, and mechanical performance for future stretchable electronic applications which would be difficult to achieve using conventional electronic materials. Although the stretchability in the reported designs are moderate, it might be possible to expand the range through optimized device structures.

■ ASSOCIATED CONTENT

S Supporting Information. Additional information on growth and transfer of graphene film and device fabrication. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Author Contributions

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