



A Numerical Study on the Mechanical Characteristics of Zinc Oxide-Based Transparent Thin Film Transistors

D.-K. Lee¹, K. Park², J.-H. Ahn², N.-E. Lee², and Y.-J. Kim^{1,*}

¹*School of Mechanical Engineering, Sungkyunkwan University, 300 Cheoncheon-dong, Suwon 440-746, Korea*

²*School of Advanced Materials Science and Engineering, Sungkyunkwan University,
300 Cheoncheon-dong, Suwon 440-746, Korea*

Zinc Oxide (ZnO) based Thin Film Transistors (TFTs) have been fabricated and analyzed to investigate mechanical characteristics regarding the stress, strain and deformation of electro circuits using the Finite Element Method (FEM). As the best compromise between the stretching and bending abilities, the coating thickness of SU-8 can be as important for bendability as a neutral mechanical plane. The neutral mechanical plane in electro circuits was designed for obtaining flexibility, e.g., bendability, in a previous numerical study. After that, through experimental validation, we observed what degree of SU-8 thickness was attributable for improved mechanical stability. The results suggest that not only numerical but also experimental measurements of the deformation and SU-8 coating thickness in electro circuits are useful for enhancing structural stability.

Keywords: Neutral Mechanical Plane, Organic TTFT, Thin Film Transistors, Flexible Display.

Delivered by Ingenta to: Yonsei University
IP: 165.132.45.198 On: Tue, 10 May 2016 07:38:49
Copyright: American Scientific Publishers

1. INTRODUCTION

Transparent Thin Film Transistors (TTFTs) that offer mechanical stretchability can enable new applications such as electronic eye imagers on hemispherical surfaces and see-through canopy window displays, which require not only extremely high levels of bendability but also fully elastic responses to large strain deformations.^{1–4} The key challenge is system design that enables much higher levels of strain ($\gg 1\%$) that can be tolerated by conventional metal or inorganic materials, without fracture or significant degradation in the electronic properties.^{4–6} Presently, a representative example of transparent TFTs uses thin films of inorganic oxides as the semiconducting and conducting layers. Oxide semiconducting materials such as ZnO and IGZO and oxide conducting materials such as ITO have real and potential advantages over silicon-based TFTs in terms of the efficient use of backlight in LCDs or emitted light in OLEDs and high voltage, temperature and radiation tolerances.^{7–11} However, these materials have intrinsic limitations in the mechanical properties, even though their electrical and optical properties can be good. For example, the tensile fracture strains for ZnO and indium tin oxide (ITO) thin films are less than 0.03%

and 1%, respectively.^{12,13} Thus, a significant challenge is to fabricate stretchable TTFTs using oxide materials. In order to solve this problem, we use a strain-induced wavy geometry in ZnO-based TTFTs. These layouts accommodate large applied strains without fracturing the materials through changes in the amplitudes and wavelengths of the wavy structures. As a result, brittle materials such as ZnO and ITO can offer effective, end-to-end stretchability, in a manner similar to that of an accordion. As a result, in terms of stretchability, as the devices are more compressed, the satisfying amplitude of wavy patterns should be high and this phenomenon leads to enhanced deformability that gives rise to longitudinal expansion. For presenting the viewpoint of bendability, it is necessary to understand that the location of the neutral mechanical plane (NMP) where the stress becomes zero is expected to be a critical factor in determining the mechanical stability of such devices. To reduce the stress on the area for a device, the neutral mechanical plane should be positioned by controlling the thickness of the encapsulating film, e.g., SU-8. Since ZnO for the active layer is the most important layer for the transistor, the neutral plane should be positioned at that layer. However, the encapsulating effect of devices, when shrinkage phenomena occur at the manufacturing step, can diminish the stretchability. In other words, in terms of the coating thickness of SU-8, it is important to analyze the

*Author to whom correspondence should be addressed.

optimal design that yields the best compromise between the stretching and bending abilities.

In the present study, as a first step, 2D FEM simulations were run to obtain such a position of the NMP when each thickness of SU-8 was coated; then, through an experimental procedure, the more promising thickness values were identified that met the stretching and bending abilities.

2. SAMPLE PREPARATION

Figure 1 shows a schematic of the manufactured TTFT with a ZnO layer ($0.1\ \mu\text{m}$), ITO source-drain electrodes ($0.1\ \mu\text{m}$), a cross-linked SiO_2 gate dielectric layer ($0.1\ \mu\text{m}$), and electroplated ITO gate electrodes ($0.1\ \mu\text{m}$) that were fabricated on $0.5\ \mu\text{m}$ SiO_2 film. A device is composed of a pad with four bridges, as shown in Figure 1. Figure 2 schematically illustrates the steps for fabricating an array of ZnO TTFTs. To fabricate stretchable, transparent thin film transistors (TFTs), the dry transfer method was used by removing the sacrificial layer. Transparent electronics are composed of transparent materials such as ZnO, ITO, and SiO_2 for the active layer, conductor, and insulator, respectively. ZnO as a semiconductor has large band gap energy and high light transmittance. For the bottom-gate structure of ZnO-based TFTs, the sacrificial layer was deposited onto a mother substrate, such as a silicon substrate; then, a SiO_2 buffer layer, which disturbs Ge diffusion, was deposited onto the sacrificial layer by an e-beam evaporator. After deposition, an ITO film

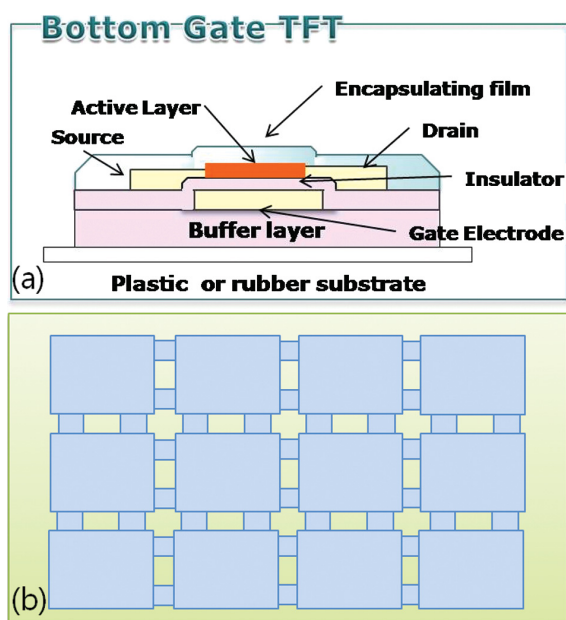


Fig. 1. Schematic showing the simulated model: (a) side view and (b) top view.

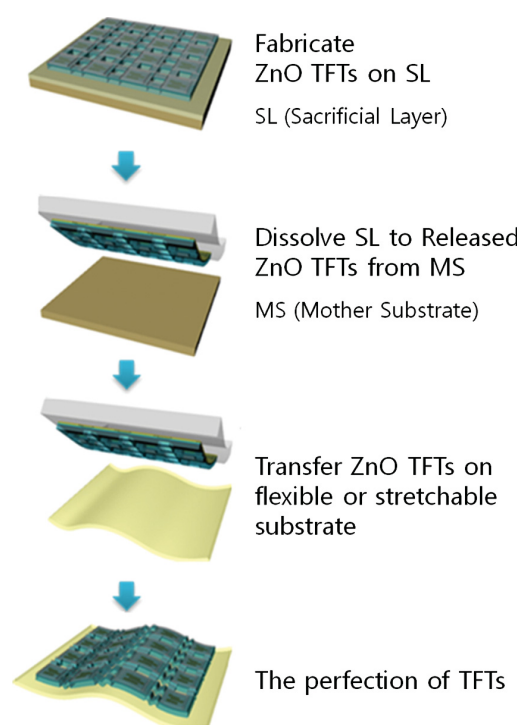


Fig. 2. Sequence of fabrication for stretchable ZnO thin film transistors.

of thickness $100\ \text{nm}$ was prepared as the gate electrode on the SiO_2 buffer layers using an RF magnetron sputtering system. Then, a $100\ \text{nm}$ SiO_2 insulator layer was deposited using Plasma-Enhanced Chemical Vapor Deposition (PECVD) equipment. Undoped ZnO for the active layer was sputtered by the RF magnetron sputtering system at room temperature and the devices were annealed at $350\ ^\circ\text{C}$ for $1\ \text{h}$ in air by using a muffle furnace to enhance the electrical properties. ITO layer deposition for the source/drain electrode was attained. The encapsulating film (SU-8) was coated by a spin coater onto the top of each device to protect the device, and the devices were revealed by a reactive ion etching (RIE) plasma system since the SiO_2 buffer layer should be exposed to the etchant. After the removal of the sacrificial layer, which has high selectivity from oxide materials, the entire device could be detached from the mother substrate using an elastomeric stamp. Then, the TFTs were transferred onto a rubber substrate that was pre-strained uniaxially. After the transfer and release, a compressive force was induced that resulted in a wavy pattern that caused the device to stretch.

3. FEM SIMULATION OF THE NEUTRAL MECHANICAL PLANE

Figure 3 shows an illuminating schematic of NMP fundamentals. The NMP defines the position where the strains

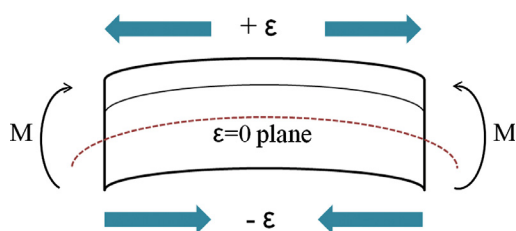


Fig. 3. Schematic of the neutral mechanical plane in fabricated thin films.

are zero ($\varepsilon_x = 0$).^{14, 15} As the following equation indicates, the multilayer stacks feature the first layer on top and the n th layer at the bottom. Their (plane-strain) moduli and thicknesses are denoted by E_1, \dots, E_n and h_1, \dots, h_n , respectively. The neutral plane is characterized by the distance, b , from the top surface, where b is given by:

$$b = \frac{\sum_{i=1}^n \bar{E}_i h_i [(\sum_{j=1}^i h_j) - h_i/2]}{\sum_{i=1}^n \bar{E}_i h_i} \quad (1)$$

The position of the neutral mechanical plane in the device structure was systematically analyzed using bending simulation. In order to reduce the stress on the area for the device, the neutral mechanical plane would be positioned by controlling the thickness of the encapsulating film, SU-8. Since the active layer, ZnO, is the most sensitive and fragile of all the layers as well as being a semiconductor, the neutral plane should be located at that layer. The distributions of the stresses and strains in the device structures were systematically analyzed using the finite element method (FEM). The problem-specific numerical model for simulating the stress and strain in the device was validated numerically with the use of a commercially available computational package, viz., COMSOL (Altsoft, Inc.). In order to analyze the structural loads and deformation in the xy -direction (including whole layers), the ZnO-based TTFT was developed in a 2D-structure, wherein the z -component of the strain was assumed to be zero

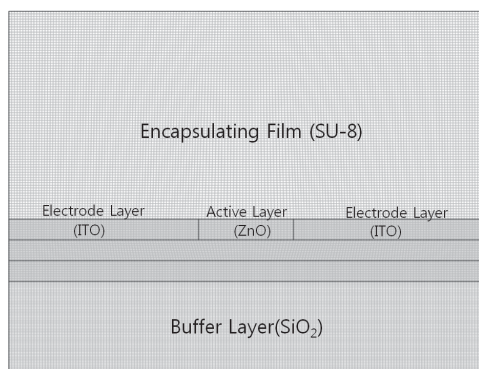


Fig. 4. Grid systems and model geometry for the finite element method.

Table I. The material parameters used in the numerical study.

| Material | Young's modulus | Poisson's ratio | Density (g/cm ³) |
|----------------------------------|-----------------|-----------------|------------------------------|
| ITO ⁽¹⁴⁾ | 116 GPa | 0.35 | 7.1 |
| ZnO ⁽¹⁵⁾ | 137 GPa | 0.36 | 5.6 |
| SiO ₂ ⁽¹⁶⁾ | 70 GPa | 0.17 | 2.2 |
| PDMS ⁽¹⁷⁾ | 1.8 MPa | 0.48 | 0.96 |

(see Fig. 3). For subsequent analysis of the stress-strain interaction, a 2D plane stress application mode was used. The lower-left and lower-right corners of the substrate were fixed in the y - and xy -directions, respectively. The structural characteristics of each device were estimated by the measurement of a forced load in the x -direction. The upper layers were analyzed as an excessively narrow region ($\sim 0.1 \mu\text{m}$ thickness) in the y -direction except for the substrate layer. To accomplish this, numerical meshes of quadrilateral elements were generated by means of the Mapped Mesh method over the entire layers. As shown in Figure 4, the number of elements in the grid system and the degrees of freedom for whole layers were 34,000 and 273,482, respectively. Each layer of thin film was modelled as a linear elastic material and the material properties of the simulated circuit are listed in Table I.^{16–19}

4. RESULTS AND DISCUSSION

The position of the neutral mechanical plane and the distributions of the stress and strain in the device structure were systematically analyzed using FEM. Figure 5 shows the numerical results for the deformation and strain distributions in the x -direction for entire layers when SU-8 was, respectively, coated and not coated on the device structure. The stress was concentrated on the ZnO layer owing to its high value of the Young's modulus in comparison with the other layers. In the y -direction, the stress distribution did not change noticeably. The results of the mechanical characteristics of a bent device indicate that SU-8 layers with different thicknesses on multi-stack hybrid layers affect the NMP position. As a result, the neutral mechanical plane in the ITO gate electrode moved to the ZnO layer, i.e., $0.65 \mu\text{m}$ of thickness from the bottom. According to the results, when the neutral plane is positioned on the active layer (ZnO), the thickness of SU-8 should be about $1 \mu\text{m}$.

Figure 6 shows the surfaces and amplitude of each device, which were measured by an optical microscope. A surface profiler was used to measure the degree of buckling under encapsulation by SU-8 that was 0.5, 0.7, 1 and $1.5 \mu\text{m}$, thick, respectively. The highest value of the amplitude implies an improvement in the stretchability. Therefore, the average values of the amplitude are listed in Table II for comparing the devices. Figure 6(a) shows that the highest amplitude is formed but the buckled region is as wide as the active layer, since a low thickness that

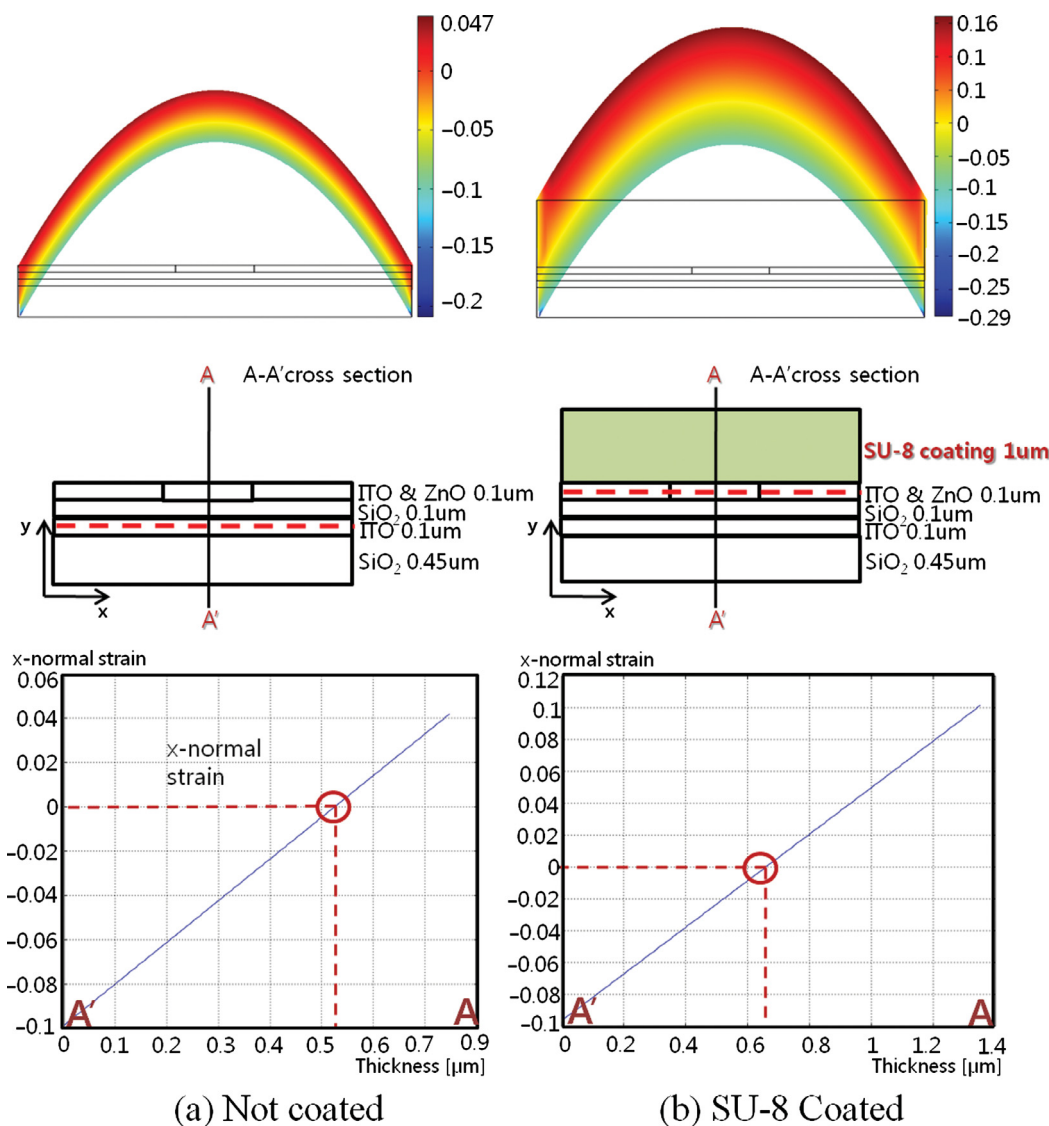


Fig. 5. Numerical results of the x -normal strain values as a function of the y -directional thickness for the neutral mechanical plane: (a) SU-8 not coated and (b) SU-8 coated with $1\ \mu\text{m}$ thickness on the ZnO layer.

performed the role of a damper layer could not endure the shrinking force. As shown in Figure 6(b), the SU-8 whose thickness was low (e.g., $0.7\ \mu\text{m}$), as in Figure 6(a), could not cause uniform wavy patterns. Figure 6(c) shows that wavy patterns are uniformly formed because of its accuracy thickness of $1\ \mu\text{m}$ —thick. The numerical results for the neutral mechanical plane of $1\ \mu\text{m}$ thickness satisfy the stretchability as the highest amplitude is formed. From Figure 6(d), it is noticeable that the thickest film can cause uniform wavy patterns but the increased stiffness brings about poor results in terms of less contraction. That is, these results show that a thickness that is either greater or lesser than $1\ \mu\text{m}$ is not appropriate for

encapsulation from the viewpoints of stretchability and bendability.

In order to design the optimal thickness of encapsulating film, the recommended ratio is analyzed in Table II. The notable feature of the optimal thickness is it causes much higher amplitude of bridges and less buckling of the pad, since these depend on the thickness of the encapsulating film, which is one of the optimal design factors. As shown in Table II, as far as the ratio of B/A is concerned, the smaller the better—we can see that the $1\ \mu\text{m}$ thickness is appropriate.

Figure 7 shows that not only the wavy pattern is almost not formed when SU-8 of $0.3\ \mu\text{m}$ thickness is coated but

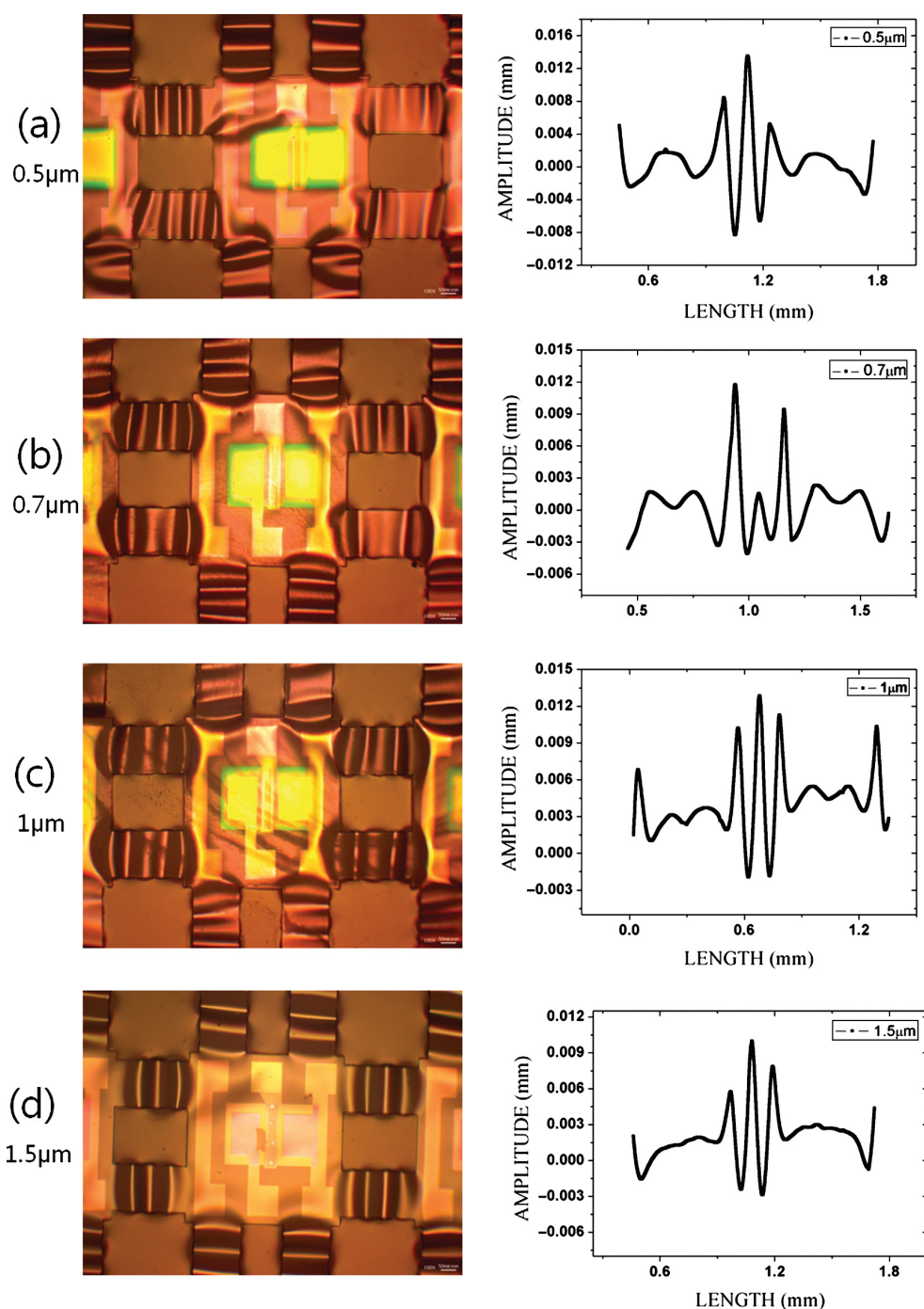


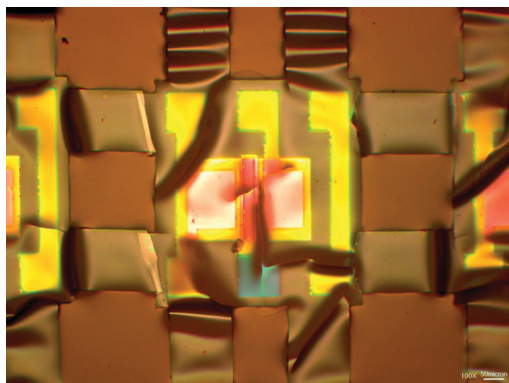
Fig. 6. Experimental results of the encapsulated devices after cooling down from 400 °C to room temperature and the measured values of the surface deformation as a function of the x -directional length: (a) 0.5 μm ; (b) 0.7 μm ; (c) 1 μm ; and (d) 1.5 μm , respectively.

also the region of buckling is entirely generated. These results can be interpreted in terms of the process of transfer (see Fig. 2) when the electrode circuits are stamped for being moved on to the PDMS. Thinner encapsulating film cannot diffuse the compression of the elastomeric

stamp (see Fig. 2) when electro circuits are detached from the mother substrate, and poor results are then caused. Therefore, it is important for the manufacturing process to achieve a high degree of accuracy, e.g., through mechanization and the avoidance of manual labor.

Table II. Relationship between the values of deformation for the optimal design.

| Film thickness (μm) | Max. amplitude of bridges: A (μm) | Max. buckling degree of the pad: B (μm) | Optimal ratio (B/A) |
|----------------------------------|--|--|---------------------|
| 0.5 | 21.9 | 40 | 1.830 |
| 0.7 | 16.6 | 26 | 1.570 |
| 1.0 | 15 | 20.5 | 1.367 |
| 1.5 | 13 | 20 | 1.540 |

**Fig. 7.** Encapsulated devices of $0.3\ \mu\text{m}$ thickness after pre-straining, as shown in Figure 6.

5. CONCLUSIONS

Several designs that meet the requirements of stretchability and bendability are proposed and compared through FEM or experimental tests. From the results of modelling, the neutral mechanical plane is found to be optimal in view of the bendability; furthermore, a thickness of $1\ \mu\text{m}$ for SU-8 encapsulating film can ensure uniform, wavy patterns for stretchability. The analytical method for optimal mechanical design can be useful in enhancing the structural stability as well as verifying the structural reliability.

Acknowledgments: Financial aid from the Korea Ministry of Education through the Brain Korea 21 Project is gratefully acknowledged. The authors are also grateful for financial support provided by the Korea Research Foundation (R01-2008-000-20533-0).

References and Notes

1. H. C. Ko, M. P. Stoykovich, J. Song, V. Malyarchuk, W. M. Choi, C. J. Yu, J. B. Geddes III, J. Xiao, S. Wang, and Y. Huang, *Nature* 454, 748 (2008).
2. G. P. Crawford, *Flexible Flat Panel Displays*, Wiley, Providence, RI (2005).
3. D. H. Kim, J. Xiao, J. Song, Y. Huang, and J. A. Rogers, *Adv. Mater.* 22, 1 (2010).
4. M.-C. Choi, M. Han, I. I. Kim, and C.-S. Ha, *J. Nanosci. Nanotechnol.* 10, 6829 (2010).
5. D. Y. Khang, H. Jiang, Y. Huang, and J. A. Rogers, *Science* 311, 208 (2006).
6. F. Spaepen, *Acta Mater.* 48, 31 (2000).
7. P. F. Garcia, R. S. McLean, M. H. Reilly, and G. Nunes Jr., *Appl. Phys. Lett.* 82, 1117 (2003).
8. R. L. Hoffman, B. J. Norris, and J. F. Wager, *Appl. Phys. Lett.* 82, 733 (2003).
9. B. I. Hwang, K. Park, H. S. Chun, C. H. An, H. Kim, and H. J. Lee, *Appl. Phys. Lett.* 93, 222104 (2008).
10. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Nature* 432, 488 (2004).
11. Y. Sun and J. A. Rogers, *Adv. Mater.* 19, 1916 (2007).
12. C. W. Ong, D. G. Zong, M. Aravind, C. L. Choy, and D. R. Lu, *J. Mater. Res.* 18, 2464 (2003).
13. Z. Chen, B. Cotterell, and W. Wang, *Engineering Fracture Mechanics* 69, 597 (2002).
14. D.-H. Kim, J.-H. Ahn, W. M. Choi, H.-S. Kim, T.-H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, and J. A. Rogers, *Science* 320, 507 (2008).
15. S.-C. Lee, D.-K. Lee, Y.-G. Seol, J.-H. Ahn, N.-E. Lee, and Y.-J. Kim, *J. Nanosci. Nanotechnol.* 11, 239 (2011).
16. D. G. Neerincx and T. J. Vink, *Thin Solid Films* 278, 12 (1996).
17. I. Ozen, M. A. Gulgun, and M. Ozcan, *Key Eng. Mater.* 264, 1225 (2004).
18. M. T. Kim, *Thin Solid Films* 283, 12 (1996).
19. H. Jiang, D. Y. Khang, J. Song, Y. Sun, Y. Huang, and J. A. Rogers, *Proceedings of the National Academy of Sciences* 104, 15607 (2007).

Received: 26 July 2010. Accepted: 22 January 2011.