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High-Performance Flexible Graphene Field Effect Transistors with Ion Gel Gate Dielectrics

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ABSTRACT A high-performance low-voltage graphene field-effect transistor (FET) array was fabricated on a flexible polymer substrate using solution-processable, high-capacitance ion gel gate dielectrics. The high capacitance of the ion gel, which originated from the formation of an electric double layer under the application of a gate voltage, yielded a high on-current and low voltage operation below 3 V. The graphene FETs fabricated on the plastic substrates showed a hole and electron mobility of 203 ± 57 and 91 ± 50 $cm^2/(V \cdot s)$, respectively, at a drain bias of −1 V. Moreover, ion gel gated graphene FETs on the plastic substrates exhibited remarkably good mechanical flexibility. This method represents a significant step in the application of graphene to flexible and stretchable electronics.

KEYWORDS Graphene, ion gel, flexible electronics, field effect transistor, low-voltage operation

Graphene has attracted attention for a range of electronic applications, such as displays, solar cells, and sensors owing to its exceptional electronic and optoelectronic properties.[1−4] Recent developments in the large area synthesis of high-quality graphene films has created new pathways for the application of graphene to high-frequency devices.[5−7] There are two general approaches for fabricating graphene devices over large areas: one that employs graphene grown directly on SiC wafers[8] and another that transfers graphene films synthesized on metal layers to other useful substrates.[9,10] The latter approach is attractive because of the special attributes of graphene films, such as flexible/stretchable device fabrication and the possibility of fabrication over large areas. This approach has produced device arrays on rigid insulating wafers and is scalable to a wafer size.[9] Although several studies have reported graphene field-effect transistors (FETs) on a plastic substrate,[11] there are still significant challenges in fabricating large scale, flexible graphene FETs.

Exploring graphene for flexible electronics requires solution-processable, high-capacitance gate dielectrics that can form at low temperature with a good interface with the graphene films transferred to plastic sheets. Although several high-k inorganic dielectrics, such as HfO_2, Al_2O_3, and ZrO_2, have been applied to the fabrication of graphene FETs, they cannot be available for flexible devices based on plastic substrates due to their high growth temperature.[8,12,13]

This paper reports a promising method for fabricating a low-voltage operating graphene FET array on plastic substrates using an ion gel as the gate dielectric. The ion gel consists of a room temperature ionic liquid and gelating triblock copolymer, which exhibits an extremely high capacitance of 5.17 $\mu F/cm^2$.[14−16] The high capacitance of the ion gel gate dielectrics in the graphene FETs provides both high on-current and low voltage operation. Furthermore, ion gel gated graphene FETs fabricated on plastic substrates show very good mechanical flexibility.

Before the fabrication of flexible graphene FETs on plastic substrate, we built typical bottom-gated graphene FETs on a SiO_2/Si wafer and top-gated devices with ion gel gate dielectrics, to examine the performance of graphene films and compare the characteristics of SiO_2 and ion gel dielectrics. Figure 1a shows the transfer characteristics (I_D-V_G) of the graphene FETs fabricated on the SiO_2 dielectrics ($t \sim 300$ nm). The channel width (W) and length (L) were 10 and 20 μm, respectively. The graphene films were synthesized by a chemical vapor deposition (CVD) method;[9,17] the detailed procedure will be explained later. The hole and electron mobility were calculated from the linear regime of the transfer characteristics using

$$I_D = \mu \frac{W}{L} C_i V_D (V_G - V_{th})$$

where C_i is the specific capacitance of the dielectric, V_{th} is the threshold voltage, and μ is the field-effect mobility. The calculated hole and electron mobility were 828 ± 58 and 189 ± 42 $cm^2/(V \cdot s)$ at $V_D = -1$ V, respectively. In addition, electron conduction of the graphene FETs was quite weak

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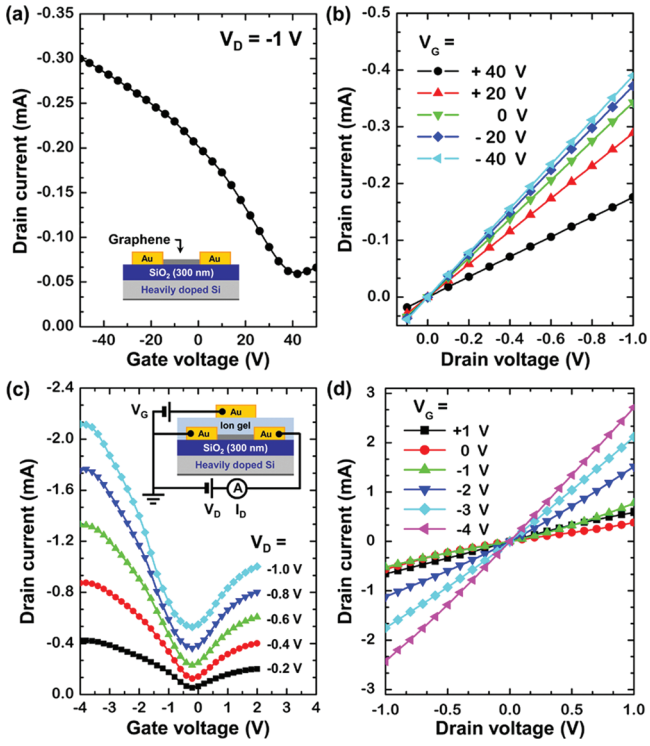

FIGURE 1. Electrical properties of graphene FETs fabricated on a rigid substrate. (a) Current−voltage transfer characteristics of the bottom-gated graphene FETs on SiO_2/Si wafer at a drain−source bias of $V_D = -1$ V. The inset indicates the geometry of the graphene FETs. The channel width and length of the device were 10 and 20 μm, respectively. (b) Output characteristics of the devices at five different gate voltages. (c) Transfer characteristics of top-gated graphene FETs with ion gel gate dielectrics at five different V_D. Inset shows the geometry of ion gel gated graphene FETs. (d) Output characteristics of ion gel gated devices.

and the Dirac point was approximately +40 V. Such asymmetry in the mobility of the two carrier and the shift in the Dirac point can be explained by the different scattering cross sections for electrons and holes and the electric fields created by charged impurities on the SiO_2 substrate, respectively.[18−20] Figure 1b shows the output characteristics (I_D−V_D) of the SiO_2-gated graphene FETs at five different gate voltages (V_G). The device showed a clear increase in conductance induced by the gate voltage and completely linear behavior, which is typical for metal/zero band gap semiconductor junctions.

The gate dielectric is the key element of graphene devices because of its important role in determining the operating voltage range. Although HfO_2 or Al_2O_3 formed by atomic layer deposition (ALD) are natural choices, the thermal limitation of plastic substrates has impeded the use of ALD processes. Ion gel gate dielectrics with high capacitance that can be formed at low temperatures can serve as robust gate dielectrics in graphene transistors. Ion gels provided a specific capacitance of 5.17 μF/cm^2 at 10 Hz, which was much larger than the typical values for 300 nm thick SiO_2 dielectrics (we will explain the ion gel dielectric formation later). This extraordinary high capacitance of the ion gel is due to the formation of an electric double layer, only nanometers in thickness, at both the ion gel/

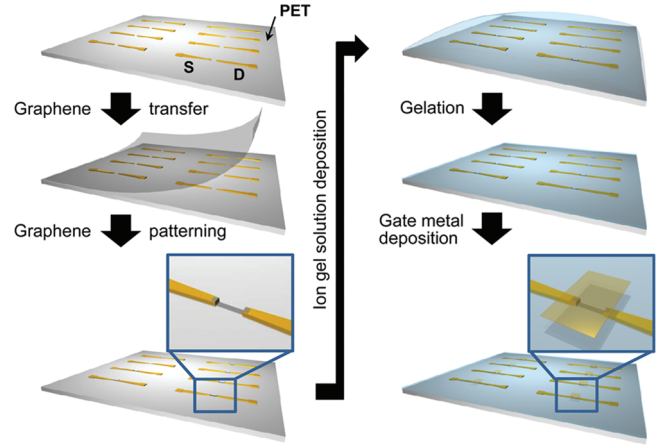

FIGURE 2. Schematic diagram of the steps used to fabricate the ion gel gated graphene transistor array on a plastic substrate.

graphene and ion gel/gate electrode interfaces under an electric field. Figure 1c shows the transfer characteristics of the top-gated graphene transistors fabricated using ion gel gate dielectrics at five different V_D. Characteristic V-shaped ambipolar behavior was obtained, where a positive and negative V_G region represents electron and hole transport, respectively. The average hole and electron mobility were 320 ± 35 and 135 ± 26 cm^2/(V·s) at $V_D = -1$ V, respectively. This decrease in carrier mobility of the ion gel gated graphene transistors may be due to two effects. One is the polymer residue that remains on the graphene surface after the transfer printing of graphene on the substrate. The other is the surface roughness of the graphene films; the graphene/ion gel interfaces are rougher than the graphene/SiO_2 interfaces. Moreover, compared to SiO_2 gate dielectrics, the asymmetric factor between hole and electron conduction decreased dramatically and the Dirac point shifted to almost zero because the counterions in the ion gel neutralize the charged impurities trapped on the SiO_2 substrate.[19,20] The output characteristics of the ion gel gated graphene transistors in the device showed reasonable drain current modulation with V_G (Figure 1d). The drain current at $V_G = -4$ V and $V_D = -1$ V was approximately 2.4 mA. This is much higher than that of SiO_2-gated transistors (~0.4 mA at $V_G = -40$ V and $V_D = -1$ V) and is a direct result of the large capacitance of the ion gel gate dielectrics.

A key advantage of graphene lies in its extremely attractive mechanical properties, which are essential for achieving flexible and stretchable electronics.[1,4,5] To demonstrate such attributes of graphene, an ion gel gated graphene FET array was fabricated on a flexible poly(ethylene terephthalate) (PET) sheet. Figure 2 shows a schematic diagram of the fabrication steps of the ion gel gated graphene transistor array on a plastic substrate. In the first step, large-area, high-quality graphene films were grown on a rectangular piece of Cu foil (25 μm thick) using the procedures described elsewhere.[9,17] Mainly mono- and bilayers of graphene were grown on the Cu foil. Poly(methyl methacrylate) (PMMA) polymer supports were coated on the graphene films on the metal layers to allow the transfer of graphene films from the Cu foil to the plastic substrate. The

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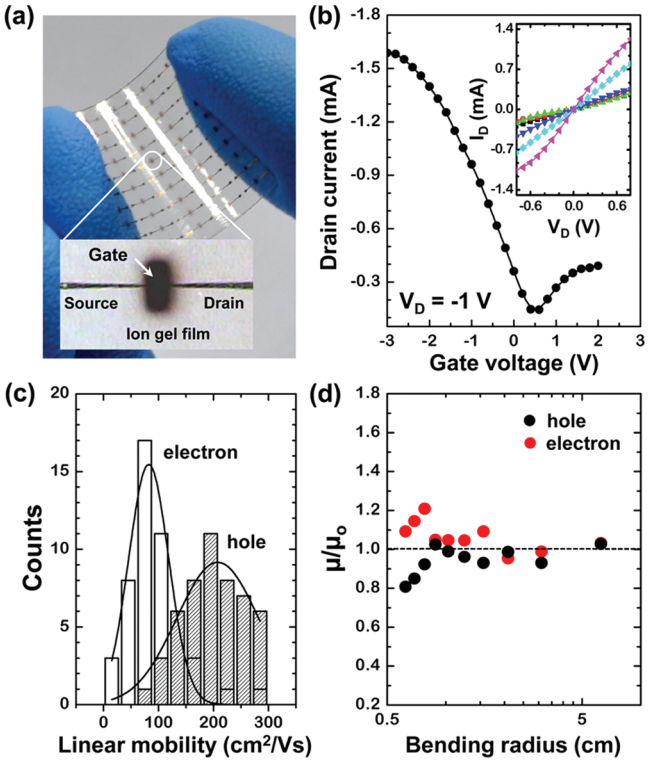

FIGURE 3. Electrical and mechanical properties of ion gel gated graphene FETs fabricated on a flexible plastic substrate. (a) Optical images of an array of devices on a plastic substrate. (b) Transfer and output characteristics of graphene FETs on plastic substrate. In output curve, the gate voltage was varied between +2 and −3 V in steps of −1 V. (c) Distribution of the hole and electron mobility of graphene FETs. (d) Normalized effective mobility (μ/μ_o) as a function of the bending radius.

supports adhering to the foil were then soaked with wet etchants to remove the metal layers. These films were then delivered by transfer printing to a PET sheet containing the source and drain electrodes (Cr/Au, 10 nm/60 nm) formed by thermal evaporation. The device patterns of the graphene films were formed by photolithography and reactive ion etching (RIE) with O_2 plasma. For ion gel gate dielectric formation, poly(styrene-*block*-methyl methacrylate-*block*-styrene) (PS-PMMA-PS) triblock copolymer and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) ionic liquid were dissolved in methylene chloride at a 0.7:9.3:90 ratio (w/w) and then drop-casted onto a graphene pattern with an Au source and drain contact. After the solvent was removed, an ion gel film was formed through physical association of the PS blocks in ionic liquid. The top gate electrodes (Au, 100 nm) were evaporated thermally through shadow masks.

Parts a and b of Figure 3 show the flexibility of the resulting device substrate as well as the transfer and output characteristics of the graphene FETs on PET. There were no significant differences in the mobility and on-current compared to that fabricated on the Si wafer. It is evident that the device operates at low voltage (<−3 V) with a high on-current, and the Dirac point is almost zero. Figure 3c shows the distribution of the hole and electron mobility of graphene FET arrays (total ∼50 devices) on PET. A Gaussian fit indicates a hole and electron mobility of 203 ± 57 and 91 ± 50 $cm^2/V \cdot s$, respectively, at a drain bias of −1 V. All measurements were performed under ambient conditions.

Mechanical flexibility and robustness are important characteristics for the application of graphene FETs in flexible electronics. A symmetric bending test was performed on the graphene FET array. Figure 3d shows the change in effective carrier mobility, normalized to the value of the graphene FETs under the unbent condition. Only 20% changes in μ/μ_o were observed as the bending radius was changed from 6 to 0.6 cm.

In summary, graphene films combined with ion gel dielectrics provide an important route to mechanically flexible, high-performance, and low-voltage graphene devices. Graphene technology may create opportunities for devices requiring unusual form factors, such as mechanical flexibility or stretchability.

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