Low Temperature Aluminum Oxide Gate Dielectric on Plastic Film for Flexible Device Application

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The growth of low temperature aluminum oxide gate dielectric on a plastic substrate is explored for flexible device application. Single-crystal-transferred-silicon is used as a channel layer. A plasma-deposited interfacial oxide layer is found beneficial for better device performances. Additional forming gas annealing also improved contact resistance and resulted in better passivation of defect sites, hence, enhanced performances. High mobility, high on current with large on–off ratio and low threshold voltage was achieved. The flexibility of the device is also reported. Devices show nearly no changes in electrical properties after bending the device to a strain value of up to 0.3%, corresponding to a bending radius of 4 mm. © 2010 The Japan Society of Applied Physics

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1. Introduction

For flexible devices on plastic films, it is necessary to grow dielectrics at relatively low temperature compared with those of conventional silicon (Si) devices owing to temperature stringency associated with plastic sheets. On the other hand, for high mobility devices, there is no alternative but to use a single-crystal channel layer as an active layer. Si transferred onto a plastic sheet is an attractive alternative for fabricating high-performance flexible device.[1,2] In addition, industries can be benefited from the vast knowledge from the conventional Si technology. Even though a transferred device with silicon dioxide (SiO_2) as a gate dielectric was previously reported,[3] in this work, atomic-layer-deposited (ALD) aluminum oxide (Al_2O_3) gate dielectric is deposited on a single-crystal transferred-silicon-ribbon onto the plastic polyamide (PI) film. Oxides grown at low temperatures usually has many defect sites.[4,5] The use of interface SiO_2 and additional annealing steps are among the few alternatives to improve device properties. After the dopant activation annealing on silicon-on-insulator (SOI) wafer, the patterned Si layer can be transferred onto plastics by poly(dimethylsiloxane) (PDMS) stamping process.[1]

In this study, Al_2O_3 was deposited by the ALD process at a low temperature. Two different approaches have been taken during the deposition process. The transistor properties improved with the inclusion of an interface oxide layer and with an additional annealing step. The mechanical flexibility of the device is also evaluated.

2. Experimental Procedure

After defining the doped region on a SOI wafer, the phosphorous (P509) spin-on dopant was used for convenience. The doping concentration was measured to be $2 \times 10^{18}\,cm^{-3}$ after activation annealing at 950 °C. After the etching of the underneath SiO_2 layer, 290 nm of the top Si layer can be transferred onto the PI sheet by the PDMS stamping process. Al_2O_3 was deposited as a gate dielectric in two different chambers using water as oxygen (O_2) precursor source and O_2 plasma as the O_2 source. The samples with water and plasma as the O_2 sources are referred to as S1 and S2 respectively throughout this paper.

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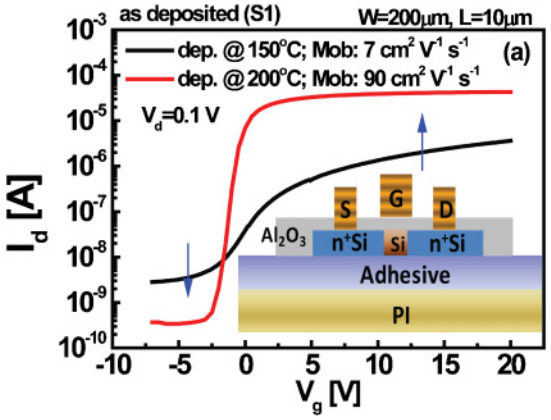

Fig. 1. (Color online) Transfer curve for ALD Al_2O_3 (S1) grown at 150 and 200 °C. The transistor performance shows significant improvement at a higher temperature. The inset shows schematic diagram of the device structure fabricated for this study.

Deposition temperature was varied from 150 to 200 °C. The thickness was ~77 nm and the dielectric constant was in the range of ~7.3 to 7.8, as determined by capacitance-voltage measurement. After source–drain–gate patterning, platinum of ~100 nm thickness was deposited as an electrode and the lift-off process was adopted. The inset in Fig. 1 shows the schematic cross-sectional view of the top-gate device structure on a PI sheet. The channel width was 200 μm with channel length varied from 10 to 25 μm. To improve the metal contact, a forming gas annealing process (FGA; H_2 = 3 wt %, remaining N_2) was performed at 200 °C at 1 atm pressure for 1 h. A computer controlled bending test module was used for the bending test of the PI sheet.

3. Results and Discussion

The effect of deposition temperature on the Al_2O_3 device was first explored. Figure 1 shows the comparison of the transfer curves of the ALD S1 devices at 150 and 200 °C. A significant improvement of device performance at a higher temperature was observed. Mobility increases from 7 to 90 $cm^2\,V^{-1}\,s^{-1}$ at a higher temperature. However the transistor shows the depletion type of behavior with negative threshold voltage (V_{th}), which implies that the transistor is in the "on state" at zero voltage. To improve the properties, another

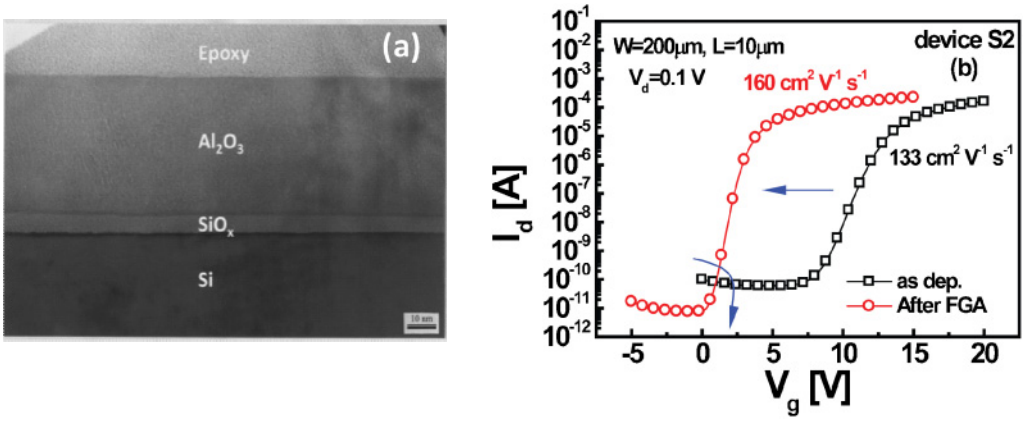

Fig. 2. (Color online) (a) TEM image of sample S2 with interfacial SiO_2 at the Si interface. (b) Transfer characteristics of sample S2 before and after FGA. After FGA, V_{th} decreases significantly, as shown in the figure.

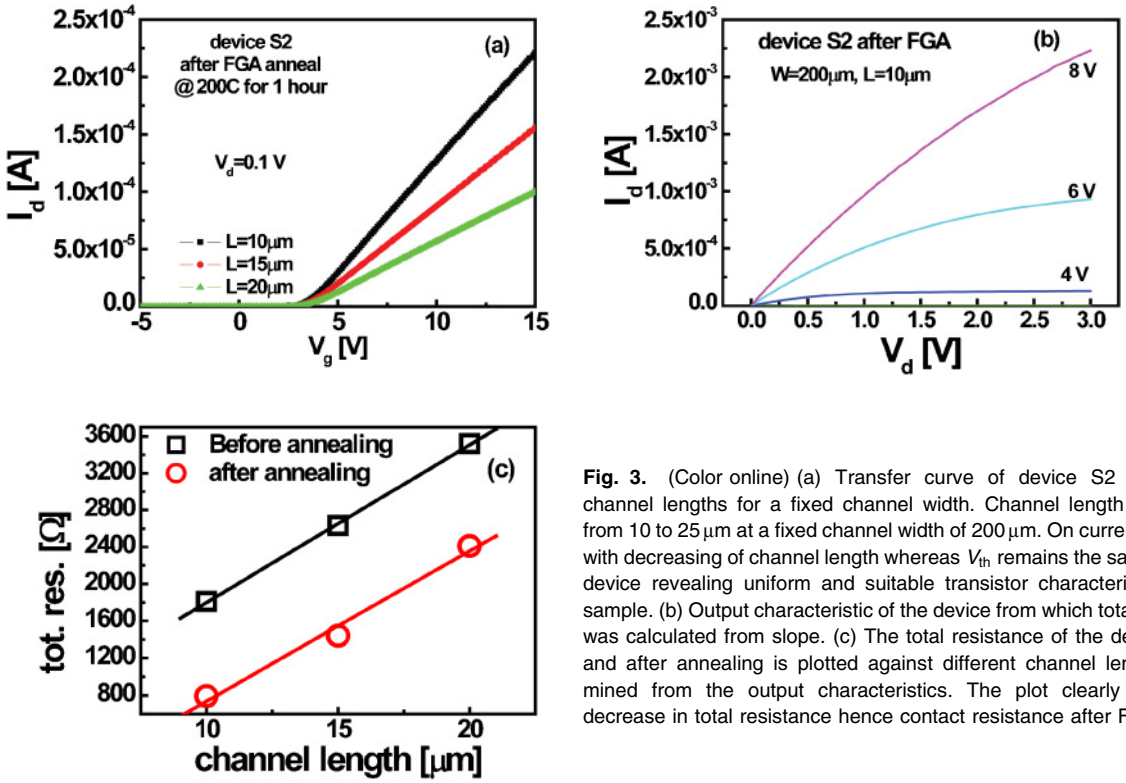

Fig. 3. (Color online) (a) Transfer curve of device S2 at different channel lengths for a fixed channel width. Channel length was varied from 10 to 25 μm at a fixed channel width of 200 μm. On current increases with decreasing of channel length whereas V_{th} remains the same for each device revealing uniform and suitable transistor characteristics of the sample. (b) Output characteristic of the device from which total resistance was calculated from slope. (c) The total resistance of the device before and after annealing is plotted against different channel lengths determined from the output characteristics. The plot clearly shows the decrease in total resistance hence contact resistance after FGA.

approach has been explored (S2). An interfacial SiO_x layer of approximately 10 nm has been grown *in situ* prior to Al_2O_3 deposition at 200 °C using O_2 plasma. Figure 2(a) shows a transmission electron microscopy (TEM) image. The interfacial SiO_x layer of 10 nm thickness shows a very clear boundary between the Si/SiO_x and SiO_x/Al_2O_3 layers. The interface layer improves interface roughness and provides stability of the devices. The transistor shows enhancement type of behavior with positive threshold voltage, which improves significantly after additional annealing at 200 °C. Figure 2(b) shows the transfer characteristics of device S2 before and after FGA. Even though the V_{th} for the as-deposited sample is quite high (+10 V), V_{th} can be reduced to +2.5 V with the additional annealing step. Furthermore, the off current also decreased one order of magnitude. The mobilities of the device before and after annealing, calculated using the conventional transistor equation,[6] were 133 and 160 $cm^2\,V^{-1}\,s^{-1}$, respectively. These mobilities are quite comparable to the previously reported mobility of Al_2O_3 dielectric device in conventional Si transistor process.[7,8]

Figure 3(a) shows the transfer characteristics of device S2 with different channel lengths at a fixed channel width of 200 μm. The device shows excellent uniform enhancement type of switching properties with proportional increase in current with decreasing channel length. Figure 3(b) shows the output characteristics. The total resistance of the device can be measured from the linear region of the output curve for both before and after annealing, [Fig. 3(c)]. It is a reasonable assumption that total resistance is equal to channel resistance and contact resistance. If we plot total resistance at different channel lengths, contact resistance can

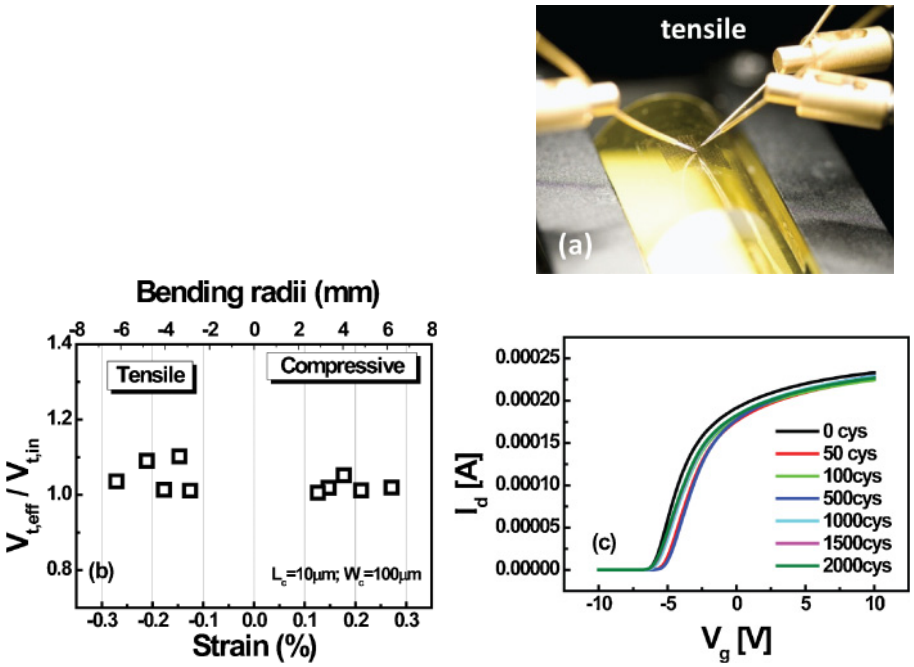

Fig. 4. (Color online) (a) Optical image of the sample on a bending (tensile state) stage. The sample was bent at different radii at both compressive stress and tensile stress and measured. (b) Relative change in V_{th} was measured at different bending radii (corresponding to different stresses). (c) Fatigue test was also performed. The transfer curve was measured after several bending cycles of up to 2000 times. The fatigue test was carried out under compressive stress, as shown in Fig. 4(a).

be calculated from the *y*-intercept. From Fig. 3(c), it can be concluded qualitatively that the contact resistance of the channel decreases after FGA.

Additionally, as the dielectric was grown at a relatively lower temperature, it contains many defect sites. H_2 from FGA can easily passivate these defects and improve the interface properties of the contacts.[9] This explains the improved electrical characteristics of the devices in terms of mobility, V_{th}, subthreshold swing, and on/off ratio.

To confirm the performance of the transistor for flexible device application it is necessary to perform electrical measurements under bending conditions. First the sample was bent on a bending stage in both compression and tension. Figure 4(a) shows an image of the sample in the tensile state on the bending stage. Figure 4(b) shows the changes of the threshold voltage unedr different stress conditions. The device was bent by varying bending radius from 2 to 6 mm, corresponding to surface strain values ranging from 0.3 to 0.1%, respectively. Both compressive stress and tensile stress were applied. V_{th} was measured from the transfer curve under each bending condition ($V_{th,eff}$) and compared with initial voltage ($V_{th,in}$) in the nonbending condition. The ratios are close to 1 implying very little change in V_{th}. Next, the fatigue test was performed after bending and straightening the device under tensile condition for several thousand cycles at the highest strain value (0.3%). Figure 4(c) shows the transfer curve measured after applying various cycles of tensile stress at a surface strain value of 0.3%. The transfer characteristics show very little change in terms of on and off current, mobility, and V_{th}.

4. Conclusions

In conclusion, the flexible device with good transistor properties has been developed with medium dielectric constant Al_2O_3 as a gate insulator. The electrical characteristics depend on deposition condition and further processing step. The device also shows excellent flexibility in terms of bending and fatigue test. Overall, the device characteristics observed in this study are very promising for future flexible display and other device applications.

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