Mechanically flexible thin film transistors and logic gates on plastic substrates by use of single-crystal silicon wires from bulk wafers

Seoung-Ki Lee,[1,2] Houk Jang,[1,2] Musarrat Hasan,[3] Jae Bon Koo,[2,3] and Jong-Hyun Ahn[1,2,a)]

[1]*School of Advanced Materials Science and Engineering, SKKU Advanced Institute of Nanotechnology, Sungkyunkwan University, Suwon 440-746, Republic of Korea*

[2]*Center for Human Interface Nano Technology (HINT), Sungkyunkwan University, Suwon 440-746, Republic of Korea*

[3]*Convergence and Component and Materials Research Laboratory, Electronics and Telecommunications Research Institute, Yuseong, Daejeon 305-700, Republic of Korea*

(Received 15 January 2010; accepted 21 February 2010; published online 26 April 2010)

This letter presents a method to fabricate single-crystal silicon wires from (100) wafer and print them onto thin plastic substrates for high-performance, mechanically flexible, thin-film transistors by dry transfer printing. Electrical measurements indicate excellent performance, with a per ribbon mobility of 580 $cm^2/V\,s$, subthreshold voltage of 100 mV/dec and on/off ratios $>10^7$. The inverter shows good performance and voltage gains of ~2.5 at 3 V supply voltage. In addition, these devices revealed stable performance at bending configuration, an important feature essential for flexible electronic systems. © *2010 American Institute of Physics*. [doi:10.1063/1.3409475]

Work over the past decade has demonstrated that semiconductor materials based on organic molecules facilitate the formation of active electronics on plastic substrates at low temperature by printing techniques.[1] The range of applications is however restricted by the performance limitations of these materials.[2] Recent research focusing on this issue explores the use of high quality, single-crystal inorganic semiconducting wire/ribbons, which can be deposited on plastic by printing process.[3–7] The top down approach using lithography and etching processes is one of general techniques for generating these printable elements.[6,7] In the simplest form, these top-down approaches begin with layered wafers such as silicon-on-insulator wafer or superlattices of GaAs/AlAs/SiGaAs in which the layers are patterned laterally and then lifted from the wafer.[8–10] However, for large-area electronics, the high cost associated with layered wafers makes this type of material source unattractive. To solve such issue, recent reports have demonstrated that Schottky barrier transistors can be formed on plastic substrates using semiconducting ribbons generated from low-cost, bulk Si (111) wafers.[11,12] However, the mobility of resulting devices is relatively low because the ohmic contact is not formed between Si and metal electrodes and Si (111) wafer has the mobility anisotropic property.[13] In this letter, we report high-performance, top gate transistors and inverter on thin plastic substrates using Si wires with heavily doped contact region fabricated from bulk Si (100) wafers through a doping, etching, and transfer printing process.

Figure 1 illustrates the fabrication steps to generate single-crystal semiconductor wires from bulk Si (100) wafers and scanning electron microscope (SEM) images. In the first step, a conventional, high-temperature doping process defines the regions to which Ohmic contacts can be formed between metal electrodes and the Si. After the photolithographic patterning of photoresist masking layers perpendicular to the $\langle 0\bar{1}1\rangle$ direction on the surface of a doped Si (100) wafer covered with SiO_2 (300 nm) deposited by plasma enhanced chemical vapor deposition (PECVD), buffered oxide etchant (BOE) removes the oxide to produce the exposed Si regions [Fig. 1(a)]. An anisotropic wet etching (20 wt % tetramethylammonium hydroxide (TMAH) solution at 100 °C) creates trenches in the exposed Si regions [Fig. 1(b)]. The head of the trench is covered with photoresist through photolithography [Fig. 1(c)]. Further isotropic reactive ion etch-

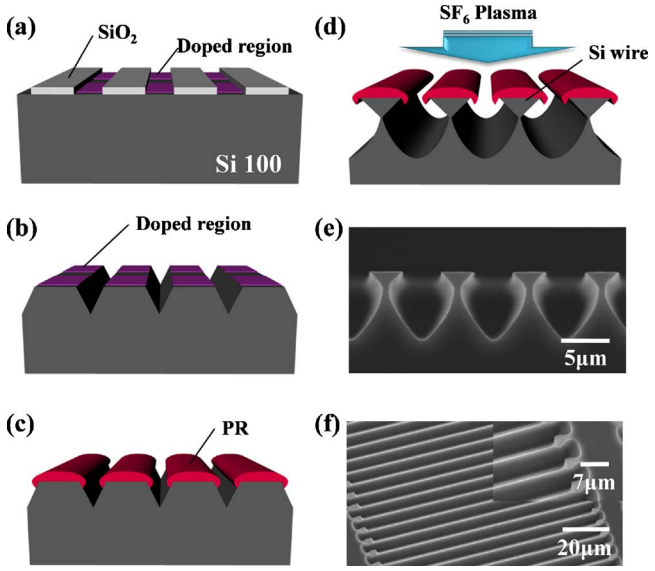

FIG. 1. (Color online) Schematic illustration of steps to generate Si wires from a bulk Si (100) wafer [(a)–(d)] and SEM images of the fabricated Si wires and the wafer surface after its lift-off [(e) and (f)]. (a) Define the doping region on a Si (100) wafer by photolithography and diffuse the dopant via rapid thermal annealing. Deposit SiO_2 by PECVD (100 nm) and remove the oxide with BOE to produce the exposed Si regions. (b) Etch the exposed Si by TMAH for trench formation. (c) Make etch mask through photolithography to protect the head of Si trench caused by SF_6 plasma during isotropic RIE process. (d) To generate freestanding Si wire, continue etching of the unprotected Si. (e) SEM image of the fabricated Si wires during RIE. (f) SEM image of the mother wafer after retrieval of the wires.

a)Author to whom correspondence should be addressed. Electronic mail: ahnj@skku.edu.

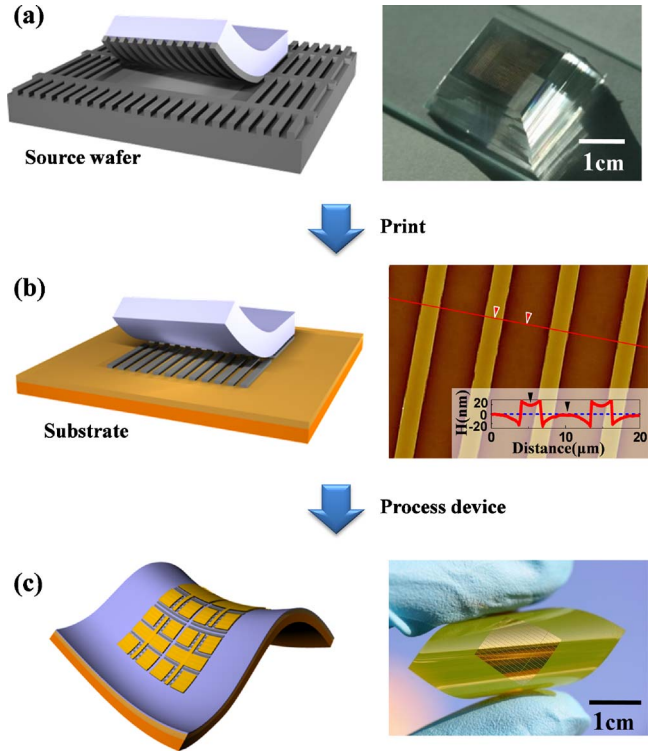

FIG. 2. (Color online) Schematic illustration of the process for transfer printing Si wire onto the desired substrates. (a) Get the freestanding Si wires from source wafer using elastomeric stamp of PDMS. (b) Arranged wires on PDMS can be transferred onto a polyimide substrate with a help of adhesive to improve bonding between the wires and substrate (left). Line-cuts through the AFM image shows the wires prominent ~20 nm from surface, indicating that the wires sank down to adhesive (right). (c) Image of generated flexible NMOSFETs on polyimide substrate.

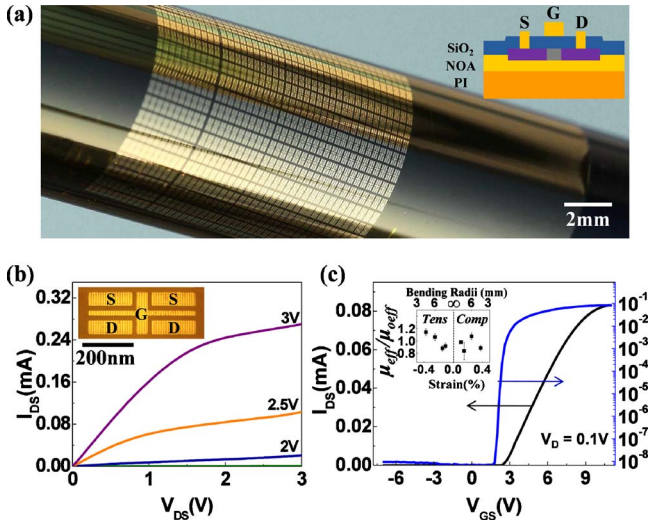

FIG. 3. (Color online) (a) Optical image and schematic cross sectional view of devices built on a polyimide substrate. (b) Typical current-voltage curves of thin film transistor device with a channel length and channel width of L_c=6 μm and W_c=160 μm, respectively. From the bottom to top, V_G varies from 0 to 3 V. The inset shows a top view of a transistor. (c) Full transfer characteristic of Si wire device, indicating a per ribbon mobility of 580 cm^2/V s, an effective device mobility of 175 cm^2/V s, subthreshold voltage of 100 mV/dec and an On/Off ratio $>10^7$ with V_D=0.1 V. The inset shows the normalized mobility (μ_{eff}/μ_{0eff}) as a function of strain induced by bending and bending radius [to 4 mm radius; 0.38% strain both tension (left) and compression (right)].

ing (RIE; etch gas: SF_6), until the Si regions meet, results in freestanding single-crystal Si wires with trianglelike cross sections [Fig. 1(d)]. The SEM image of resulting single-crystal Si wires reveals their dimensions of 2.1 μm thick, 160 μm long, and 3.0 μm wide [Fig. 1(e)]. These Si wires formed in this manner show smooth surface morphologies and good mechanical flexibility. The SEM image of handled Si(100) wafer in angled view shows the wires lift-off uniformly from source wafer and fracture cleanly at anchor region [Fig. 1(f)].

To demonstrate the utility of these Si wires as flexible devices, an array of top gate N-type metal-oxide-semiconductor field effect transistors (NMOSFETs) was fabricated. A flat elastomeric stamp of poly (dimethylsiloxane) (PDMS) with Si wires lifts the wires from the wafer by van der Waals forces between PDMS and the wires [Fig. 2(a)]. These wires on PDMS can be transferred onto a polyimide (25 μm) substrate, which is coated with UV-curable adhesive to improve bonding between the wires and substrate. Atomic force microscope (AFM) image of transferred Si wires onto a plastic substrate via a high yield printing process (>99%) reveals that the wires are well aligned without destroying the orientation and any cracking of the wires [Fig. 2(b)]. Line-cuts through the AFM image show the wire width of ~3 μm and the surface profiles of ±20 nm, indicating that the wires are deeply embedded in the adhesive and the device surface is quite flat. The gate dielectric layer consists of a layer of 100 nm thick SiO_2 deposited by PECVD. Source, drain and gate electrodes (Au/Cr: 100/5 nm) for transistor as well as the device interconnects needed to form circuits are defined in a single step by photolithography and lift-off [Fig. 2(c)].

Figure 3(a) presents optical images of an array of NMOSFETs on polyimide sheets wrapped around the cylinder bar with diameter of 10 mm and a device structure schematic. Figures 3(b) and 3(c) show the current-voltage and the transfer characteristics of a typical NMOSFET that has a channel length (L_c) of 6 μm and channel width (W_c) of 160 μm and a top view of a typical transistor [inset of Fig. 3(b)]. The devices show the on/off ratio of $>10^7$, with a threshold voltage of ~2.5 V and subthreshold voltage of 100 mV/dec. The per ribbon mobility in the linear regimes is 580 cm^2/V s (fill factor ~30%, effective device mobility ~175 cm^2/V s). These electrical performance parameters is somewhat better than those previously reported on the Schottky barrier transistors fabricated using Si (111) wafers (The per ribbon mobility ~207 cm^2/V s, on/off ratio $>10^4$, and subthreshold voltage >350 mV/dec).[11,12] To study the mechanical properties of devices, we performed bending test in the channel transport direction. The inset of Fig. 3(c) shows the result of the frontward and backward bending tests on NMOSFETs at strain values up to 0.38%, corresponding to a bending radius of 4 mm. For this range of strains, we observed only small changes in μ_{eff}/μ_{0eff} (where μ_{0eff} and μ_{eff} are the effective device mobilities in the unbent and bent states, respectively). These results suggest that the single-crystal Si wire transistors may have good flexibility properties, even at the bending radii of 4 mm.

High performance Si wire-based transistors of this type can be integrated into circuits using similar types of processing techniques. An NMOS inverter represents one of the simplest examples. Figures 4(a) and 4(b) present an image of the setup of the frontward and backward bending tests on in-

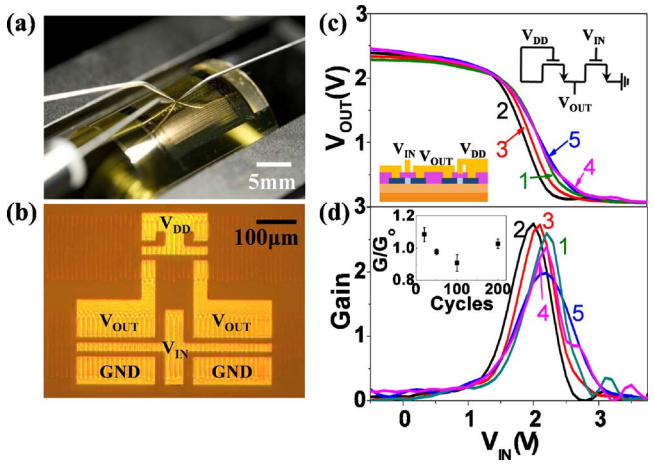

FIG. 4. (Color online) (a) Image of the setup for the bending and cycle test. (b) Image of a printed array of NMOS inverter on a PI substrate. (c) Characteristics of an inverter consisting of transistors with load to driver width ratio of 7.5, with a 3 V_{supply} at different bending radii [1: tension (0.38%), 2: tension (0.16%), 3: original state. 4: compression (0.16%), and 5: compression (0.38%)]. The inset shows a schematic illustration of the inverter (bottom) and a circuit diagram (top). (d) Gain characteristics calculated from the curves in (c). The inset shows the normalized peak gain as a function of bending cycles (to 4 mm bending radius, corresponding to ~0.38% strain).

verter at strain values up to 0.38%, and optical image of a representative NMOS inverter, respectively. The load and drive devices have W_c of 21 μm and 160 μm, respectively. The values for L_c in both cases are 10 μm. The inverter shows good performance and voltage gains of ~2.5 at 3 V supply voltage. Figures 4(c) and 4(d) show the changes in voltage transfer characteristics and the gain profiles of inverter obtained at different bending radii, respectively. The inset of Fig. 4(d) shows the variation in the normalized gain with hundreds of bending cycles. These results show slight but nonsystematic variation in electrical properties of circuits.

In conclusion, the methods described in this paper constitute a potentially low cost fabrication route for Si wires from bulk Si(100) wafers. They represent a printable form of single-crystal Si wires with properties suitable for constructing high performance devices on flexible plastic substrates. Our preliminary results suggest that individual devices of this kind can be integrated into complex circuits with functionalities appropriate for diverse applications.

This work was supported by the IT R&D program of Ministry of Knowledge Economy of Korea (MKE, Grant No. 2008-F024-01, Development of Mobile Flexible IOP Platform) and the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (Grant Nos. 331-2008-1-D00265 and 2009-0083540).

[1] S. R. Forrest, Nature (London) **428**, 911 (2004).
[2] R. H. Reuss, B. R. Chalamala, A. Moussessian, M. G. Kane, A. Kumar, D. C. Zhang, J. A. Rorers, M. Hatalis, D. Temple, G. Moddel, B. J. Eliasson, M. J. Estes, J. Kunze, E. S. Handy, E. S. Harmon, D. B. Salzman, J. M. Woodall M. Ashraf Alam, J. Y. Murthy, S. C. Jacobsen, M. Olivier, D. Markus, P. M. Campbell, and E. Snow, Proc. IEEE **93**, 1239 (2005).
[3] C. M. Lieber, Solid State Commun. **107**, 607 (1998).
[4] M. C. McAlpine, R. S. Friedman, S. Jin, K.-h. Lin, W. U. Wang, and C. M. Lieber, Nano Lett. **3**, 1531 (2003).
[5] A. Javey, S. Nam, R. S. Friedman, H. Yan, and C. M. Lieber, Nano Lett. **7**, 773 (2007).
[6] N. A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff, and J. R. Heath, Science **300**, 112 (2003).
[7] E. Menard, K. J. Lee, D. Y. Khang, R. G. Nuzzo, and J. A. Rogers, Appl. Phys. Lett. **84**, 5398 (2004).
[8] Y. Sun, D.-Y. Khang, F. Hua, K. Hurley, R. G. Nuzzo, and J. A. Rogers, Adv. Funct. Mater. **15**, 30 (2005).
[9] J.-H. Ahn, H.-S. Kim, E. Menard, K. J. Lee, Z. Zhu, D.-H. Kim, R. G. Nuzzo, and J. A. Rogers, Appl. Phys. Lett. **90**, 213501 (2007).
[10] H.-C. Yuan and Z. Ma, Appl. Phys. Lett. **89**, 212105 (2006).
[11] S. Mack, M. A. Meitl, A. J. Baca, Z.-T. Zhu, and J. A. Rogers, Appl. Phys. Lett. **88**, 213101 (2006).
[12] A. J. Baca, M. A. Meitl, H. C. Ko, S. Mack, H.-S. Kim, J. Dong, P. M. Ferreira, and J. A. Rogers, Adv. Funct. Mater. **17**, 3051 (2007).
[13] M. Yang, M. Leong, L. Shi, K. Chan, V. Chant, A. Chout, E. Gusev, K. Jenkins, D. Boyd, Y. Ninomiya, D. Pendleton, Y. Surpris, D. Heenan, J. Ott, K. Guarini, C. D'Emic, M. Cobb, P. Mooney, B. To, N. Rovedo, J. Benedict, R. Mo, and H. Ng, Tech. Dig. - Int. Electron Devices Meet. **2003**, 453.