



## Hydrogen Defect Passivation of Silicon Transistor on Plastic for High Performance Flexible Device Application

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The electrical characteristics of a transistor on a transferred silicon ribbon are demonstrated. The process temperature is limited to 200°C for potential use on plastic sheets. Additional hydrogen annealing reduces the threshold voltage and improves the transistor properties. A high mobility of around 160 cm<sup>2</sup>/V s, with a high on/off ratio and an off current of as low as <10<sup>-11</sup> A, is achieved. The flexibility of the device is evaluated after applying stress in the bended condition. The device shows very little change in properties with a bending radius <4 mm. Overall, good electrical and mechanical properties are demonstrated for future use on flexible device applications.

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Electronic devices on a flexible plastic substrate soon have a market potential in the form of flexible displays, radio frequency identification tags, solar cells, and various biosystems.<sup>1,2</sup> Many organic semiconductors,<sup>3,4</sup> oxide semiconductors,<sup>5,6</sup> and amorphous and polysilicon<sup>7,8</sup> have been used as an active semiconductor layer for a flexible device application. But due to their intrinsic limitations, it is not possible to obtain high performance devices. Hence, there is no alternative but to use a single-crystal semiconductor as an active layer. Mietl et al.,<sup>9</sup> Menard et al.,<sup>10</sup> and Ahn et al.<sup>11</sup> developed a transfer technique where after the doping process, a single crystalline silicon active layer can be transferred onto the plastic sheet from the silicon-on-insulator (SOI) wafers, which is quite attractive for a high performance transistor.

The dielectric grown at low temperatures on the plastic sheets contains many defect sites and interface dangling bonds.<sup>12,13</sup> To improve the device properties, successful defect passivation is absolutely necessary. Hydrogen (H<sub>2</sub>) passivates the defect sites far more effectively, especially near the interface region.<sup>14,15</sup> Some studies also show effective passivation even at relatively lower temperatures.<sup>16-18</sup> In this study, transistor properties with an aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) gate dielectric and platinum (Pt) as a gate electrode are presented. Properties in the bended condition are also reported.

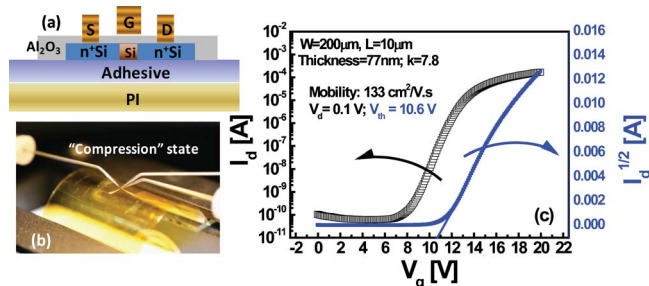
After defining the doping region on the SOI wafer, the phosphorous spin-on-dopant (P509) was used for convenience.<sup>19</sup> The doping concentration was measured to be  $2 \times 10^{18}$  cm<sup>-3</sup> after activation annealing at 950°C. After etching the underneath SiO<sub>2</sub> layer, 290 nm of the top Si layer can be transferred onto the polyimide (PI) sheet via the poly(dimethylsiloxane) stamping process. A detailed transfer process has been described elsewhere.<sup>11</sup> After the transfer process, Al<sub>2</sub>O<sub>3</sub> was deposited as a gate dielectric in a plasma-enhanced atomic layer deposition chamber at 200°C. The thickness of the dielectric was ~77 nm and that of the dielectric constant was 7.8. After the source-drain gate patterning, platinum of ~100 nm thickness was deposited as an electrode, and a lift-off process was adopted. Figure 1a shows the schematic cross-sectional view of the top-gate device structure on the PI sheet. The device width was 200 μm with the channel length varied from 10 to 20 μm. To improve the contact between the metal and source-drain, a forming gas annealing (FGA) process (H<sub>2</sub> = 3 wt % and the rest is N<sub>2</sub>) was performed at 200°C at 1 atm pressure for 1 h.

Consequently, high pressure pure H<sub>2</sub> annealing (HPHA, 20 atm, 99.99%) was also performed at 200°C. A computer-controlled bending test module was used for the bending test of the PI sheet.

Figure 1b shows the device at a compressive stress condition on the bending stage. Figure 1c shows the transfer ( $I_d$ - $V_g$ ) characteristic of the as-deposited sample both in the linear and log scale. The  $I_d$ - $V_g$  curve shows the typical n-type transistor with an enhancement mode of operation. The linear scale shows the threshold voltage ( $V_{th}$ ) of +10.8 V, which is quite high, indicating many charges and defects at the dielectric and interfaces. To reduce  $V_{th}$  and improve the interface, an additional annealing step in forming gas and H<sub>2</sub> was performed. The transfer curve is shown in Fig. 2a, in both the linear and log scale (the inset). As indicated by the arrows,  $V_{th}$  significantly reduced to 2.2 V after FGA and to 0.5 V after HPHA. The off current reduced to below 10<sup>-11</sup> A with little change in the on current. The result can be related to the better contact between the metal and the dielectric and also the defect passivation by H<sub>2</sub> near the interface and bulk oxide.

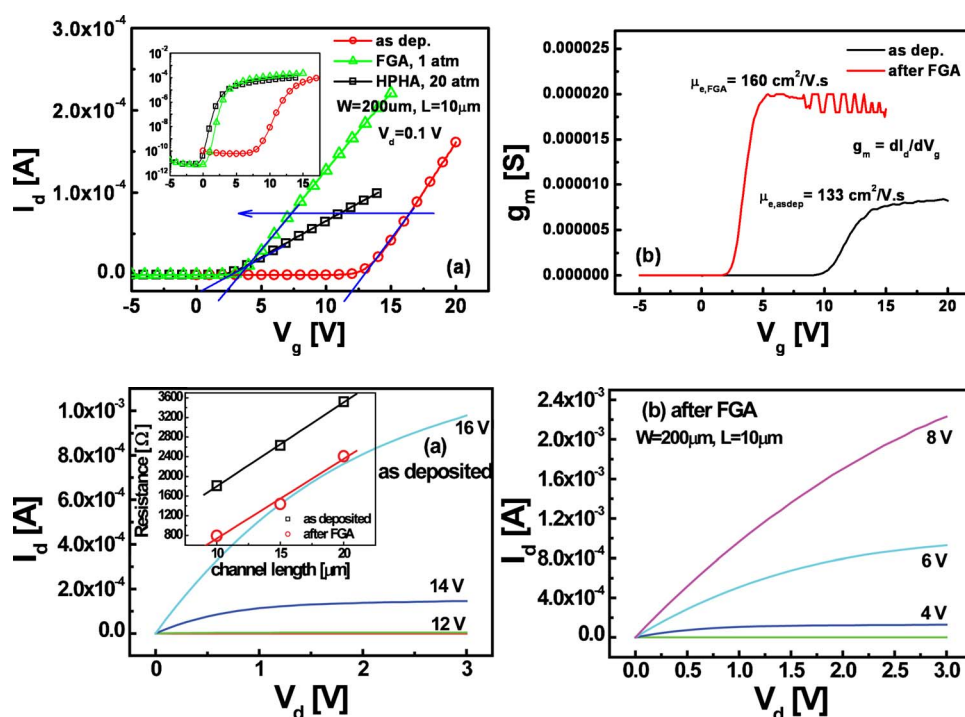
Figure 2b compares the transconductance values between both the as-deposited and FGA samples. After FGA, the  $g_m$  peak value increased from 8 to 20 μS. The corresponding effective peak mobilities for the FGA sample and the as-deposited sample are 160 and 133 cm<sup>2</sup>/V s, respectively. Figure 3 compares the output characteristics. The current increases significantly after FGA.

We measured the total resistance of our device from the output curve at different channel lengths. The total resistance can be considered to be a contribution of the channel resistance and contact



**Figure 1.** (Color online) (a) Schematic representation of the cross-sectional view of the top-gate device structure. (b) Optical image of the flexible device at the bending stage and (c) transfer characteristics of the enhancement type of n-transistor in the as-deposited condition.

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**Figure 2.** (Color online) Comparison of the (a) transfer characteristics between as-deposited, FGA, and HPHA device (inset in log scale) and (b) the corresponding transconductance curve between the as-deposited and the FGA sample.

**Figure 3.** (Color online) Output characteristics of the (a) as-deposited sample and after (b) FGA. The figure inset shows the total resistance of the devices before and after FGA.

**Table I.** Comparison of electrical properties between devices before and after FGA.

Sample condition	On/off ratio	$g_{m,max}$ ( $\mu\text{S}$ )	Mobility ( $\text{cm}^2/\text{V s}$ )	$V_{th}$ (V)	Subthreshold slope (V/dec)
As-deposited	$> 10^6$	8	133	10.8	0.7
FGA	$> 10^7$	20	160	2.20	0.36
HPHA	$> 10^7$	18	155	0.5	0.4

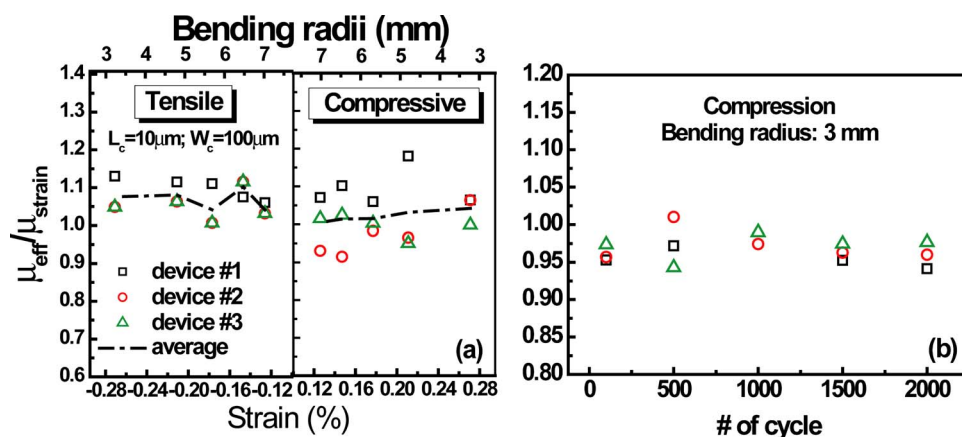
resistance. We can separate the contact resistance by plotting the total resistance at different channel lengths (inset of Fig. 3a). From the figure we can conclude that the contact resistance of the device was improved by FGA but it cannot be responsible for the large  $V_{th}$  shift alone. Further improvement can be caused by the defect passivation in both the interface and bulk sites after  $\text{H}_2$  annealing even though the annealing temperature is quite low compared to that of the conventional method.

Table I summarizes all the electrical properties that have been

discussed so far. The mobility values presented here are quite low compared to  $\text{SiO}_2$  but are comparable to the reported  $\text{Al}_2\text{O}_3$  transistor on conventional complementary metal oxide semiconductor technology.<sup>20,21</sup>

Next, the flexibility of the device was tested at different bending radii ( $R_c$ ). The ratio of the device mobility before and after bending against the bending radius and the corresponding strain values is plotted in Fig. 4a for each of the three devices and their averages. Very little degradation of mobility has been observed at  $R_c = 0.271$  mm corresponding to  $< 0.3\%$  strain. Figure 4b shows the fatigue test after several cycles of bending at a bending radius of 3 mm (compressive stress).

In conclusion, a flexible transistor device with excellent flexibility has been demonstrated to have high mobility and low threshold voltage. Low off current, high on-off ratio, and high mobility have been achieved. The exact mechanism for improved device performance after annealing requires a much more detailed study, but better contact resistance and dielectric quality are responsible for better device properties. Additional  $\text{H}_2$  annealing is very promising for future flexible device application.



**Figure 4.** (Color online) (a) The mobility change in the devices at different bending radii (the smaller the radius, the larger the strain). (b) The normalized mobility after several cycles of bending. Both cases of mobility show very little change.

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