Self-assembled nanodielectrics and silicon nanomembranes for low voltage, flexible transistors, and logic gates on plastic substrates

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This letter reports the fabrication and electrical characterization of mechanically flexible and low operating voltage transistors and logic gates (NOT, NAND, and NOR gates) using printed silicon nanomembranes and self-assembled nanodielectrics on thin plastic substrates. The transistors exhibit effective linear mobilities of ~ 680 $cm^2/V\,s$, on/off ratios $>10^7$, gate leakage current densities $<2.8\times10^{-7}$ A/cm^2, and subthreshold slopes ~ 120 $mV/decade$. The inverters show voltage gains as high as 4.8. Simple digital logic gates (NAND and NOR gates) demonstrate the possible application of this materials combination in digital integrated circuits. © *2009 American Institute of Physics*. [doi:10.1063/1.3256223]

With suitable design strategies, inorganic semiconductors can be used in mechanically compliant electronics for applications in areas, such as biomedical and bioinspired devices, lightweight/rugged electronics, and advanced communication and sensor systems, where conventional wafer-based technologies cannot meet requirements.[1–5] We and others have demonstrated mechanically flexible and stretchable electronic devices such as metal-oxide-semiconductor thin-film transistors (MOS-TFTs) and various analog and digital integrated circuits (ICs) using single crystalline silicon micro/nanomembranes and ribbons (which we refer to as microstructured silicon, μs-Si) as building blocks.[1,2,6] A key element of these devices is the gate dielectric, due to its important role in determining the operating voltage and subthreshold characteristics. Although SiO_2 is a natural choice, temperature limitations associated with organic substrates frustrate the use of standard deposition procedures. Low temperature plasma-enhanced deposition provides a route to good, although not ideal properties.[1] As a result, besides the semiconductor itself, the material for the gate dielectric is the most challenging aspect of these systems. Recent research indicates that self-assembled nanodielectrics (SANDs), deposited at low temperatures, can serve as robust, low-leakage gate dielectrics in TFTs fabricated with a range of organic,[7] nanotube,[8] and amorphous or polycrystalline inorganic thin-film semiconductors such as ZnO,[9] In_2O_3,[10] and CdSe[11] with exceptionally low leakage and excellent switching properties. This letter illustrates the utility of SANDs as gate dielectrics in μs-Si devices including n-channel MOS (NMOS) TFTs, inverters, and various logic gates on thin polyimide (PI) substrates.

The fabrication begins by creating degenerately doped contact regions on p-type silicon-on-insulator wafers (150 mm SOITEC UNIBOUND; 300-nm-thick top silicon layer; resistivity=13.5–22.5 Ω cm, and 1000-nm-thick buried oxide layer) via phosphorous diffusion using a spin-on-dopant (P509; Filmtronics) and procedures described elsewhere.[12] Photolithography and reactive ion etching define the lateral dimensions of silicon nanomembranes (i.e., the form of the μs-Si) that are released from the wafer by etching the buried oxide with hydrofluoric acid, as illustrated in Fig. 1(a). As a source of μs-Si, bulk wafers can also be used.[13] Transfer printing next delivers these membranes onto a PI sheet (70-μm-thick) coated with a thin, spin-cast layer of a liquid PI precursor (Sigma Aldrich) which serves as an adhesive.

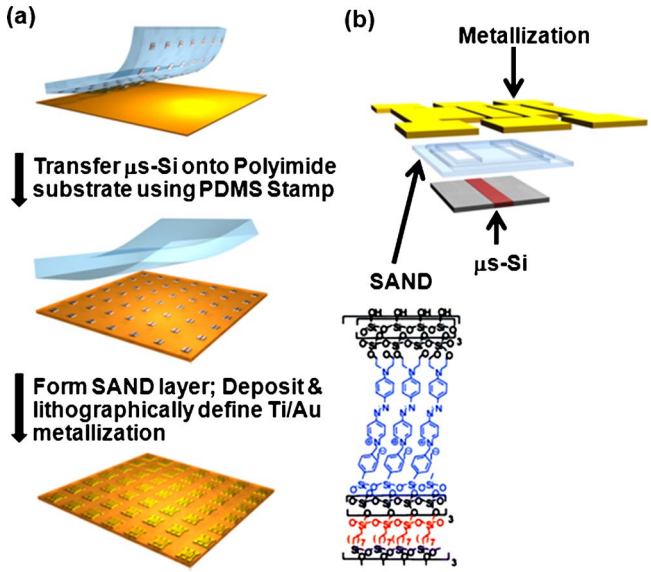

FIG. 1. (Color online) (a) Schematic illustration of the fabrication process for μs-Si TFTs with SAND gate dielectrics. (b) Layout of the device, in an exploded layer-by-layer schematic view. The chemical structure of the SAND used here appears below.

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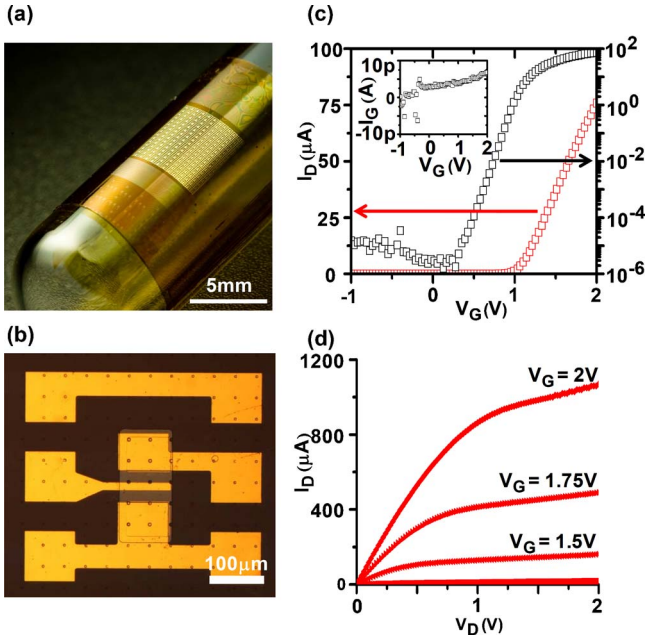

FIG. 2. (Color online) (a) Optical image of an array of μs-Si TFTs with SAND dielectrics on a PI (75-μm-thick) substrate, wrapped around the test tube with diameter of 12 mm. (b) Optical images of an individual device. (c) Drain current (I_D) as a function of gate voltage (V_G) in both linear (gray) and logarithmic (black) scale, measured with source/drain bias (V_D) of 50 mV. The inset shows the gate leakage current for V_G between −1 and 2 V. (d) Drain current as a function of source/drain bias for various gate biases, for a typical device.

Self-assembled nanodielectrics (SANDs; ~15 nm thick) deposited[9] on the native oxide of the exposed membrane surfaces serve as gate dielectrics for the NMOS TFTs. The type of SAND used here consists of alternating organic layers (saturated alkyl and π-stilbazolium) strongly interconnected by glassy siloxane networks that planarize the surface and enhance structural integrity by cross-linking and filling pinholes. This SAND multilayer exhibits a capacitance of ~180 nF/cm^2.[9] Etching defines openings in the SAND and native oxide for source and drain metallization. Photolithography and liftoff then define Ti/Au (10/150 nm) for source, gate, and drain electrodes, as well as for interconnects between transistors for logic gates.

Figure 2 provides optical images and electrical characterization data for representative NMOS TFTs. As shown in Fig. 2(b), the devices have channel lengths and widths of 7.5 and 100 μm, respectively. Figure 2(c) presents a plot of the transfer characteristic in both linear (red) and logarithmic (black) scales where output (drain) current is plotted as a function of the input (gate) bias voltage for a fixed output (drain) voltage of 50 mV. The effective device mobility in the linear regime can be extracted from these data using a parallel plate capacitance model and standard analysis procedures.[14] The mobility for the device shown is $\sim 680 \pm 50$ cm^2/V s, and the on/off ratio is $>10^7$. Device-to-device variation in the mobility is ~10%, within the processing variation and measurement error typically observed. The leakage current to the gate through the SAND layer is <7 pA throughout the entire gate bias range (from −1 to 2 V) and is about 3.9 pA at 1 V, corresponding to leakage current densities of $<2.8\times10^{-7}$ and $\sim 1.5\times10^{-7}$ A/cm^2, respectively. These values are near the noise limit of our instrumentation; see inset of Fig. 2(c). The threshold voltage (V_{th}) and subthreshold slope (S), also extracted from the transfer characteristics, are $\sim 1.1 \pm 0.05$ V and $\sim 120 \pm 4$ mV/decade, respectively. The observed variations in threshold voltage and the subthreshold slope are ~4% and 3%, respectively; both are within the measurement error that we typically observe. These performance parameters (effective device mobility, on/off ratio, and subthreshold slope) are all somewhat better than those previously reported on similar devices using a SiO_2 gate dielectric deposited at 250 °C by plasma-enhanced chemical vapor deposition (PECVD) (effective device mobility ≈600 cm^2/V s, on/off ratio ≈10^5, and subthreshold slope ≈230 mV/decade with 100 nm of SiO_2 dielectric layer).[1] More important than these differences is that SAND materials offer much more attractive processing conditions than PECVD SiO_2. In particular, SANDs can be deposited near room temperature using solution processing, whereas PECVD SiO_2 requires higher temperatures and vacuum conditions. Figure 2(d) shows current-voltage data, indicating output resistances of 6.2, 13.4, 34.3, and 133.7 k Ω at gate biases of 2, 1.75, 1.5, and 1.25 V, respectively.

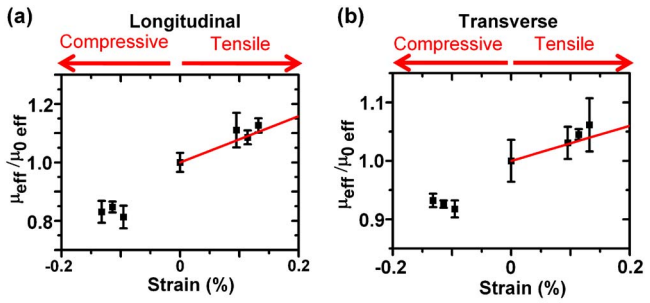

FIG. 3. (Color online) Normalized effective mobility as a function of bending-induced strain in the (a) longitudinal direction. (i.e., along the channel direction) (b) transverse direction (i.e., perpendicular to the channel direction). The gray lines correspond to independent measurements on wafer-based devices with similar dimensions.

To investigate the mechanical properties, we performed bending tests in the longitudinal (i.e., along the channel transport direction) and transverse (i.e., perpendicular to the longitudinal case) directions by measuring the electrical characteristics of the devices while wrapped on tubes having different circular cross-sections. This bending induces strain in the silicon, which can change the intrinsic mobility, as is well known.[15] Figure 3 shows the effective device mobility as a function of applied tensile and compressive strains in longitudinal and transversal directions, where the strain is computed from a mechanical analysis presented elsewhere.[16] The effective device mobilities were evaluated at calculated strains of 0.1%, 0.11%, and 0.13% which corresponds bend radii of 8.80, 7.35, and 6.35 mm, respectively. These variations are comparable to those observed by Zhao *et al.*,[17] where the effects of uniaxial tensile strain were studied on partially depleted SOI MOSFETs with device dimensions comparable to ours. These results appear as a solid line in Fig. 3. The effective device mobility increases under tensile strain and decreases under compressive strain.[17,18]

To demonstrate the applicability of SAND-based μs-Si transistors for circuit applications, we fabricated the three logic gates (NOT, NAND, and NOR gates) that are the essential building blocks of digital ICs. Other types of Boolean logic gates and higher level digital ICs (i.e., latches, flip flops, arithmetic logic unit, etc.) can be realized from a network of these logic gates. In all cases, we used NMOS for

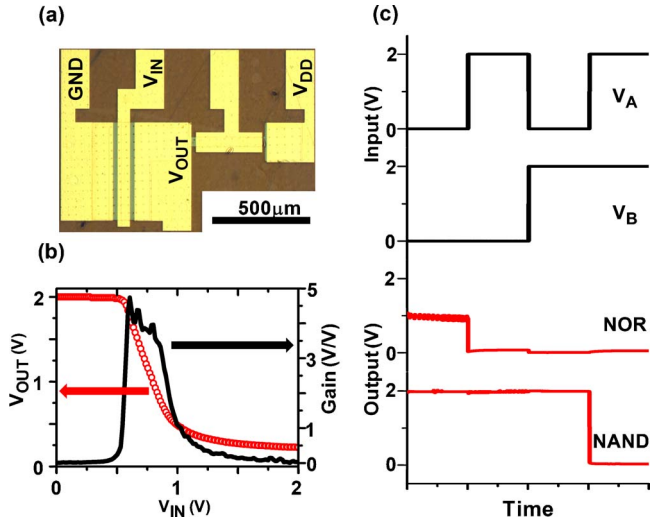

FIG. 4. (Color online) (a) Optical Image of an inverter based on μs-Si TFTs with SAND gate dielectrics. All logic gates (NOT, NAND, and NOR) are biased with V_{DD}=2 V and GND (0 V). (b) VTC of an inverter (gray), and Gain (black). (c) Output characteristic of a NAND gate and a NOR gate. V_A and V_B represent the input voltages and V_{OUT} represents the output voltage.

both pull-up and pull-down transistors, placing them in the category of enhancement-load NMOS logic.[19] Both the supply voltage (V_{DD}) and the input voltage (V_{IN}) were limited to 2 V, to demonstrate the possibility of low-voltage operation. Figure 4(a) shows an optical image of a representative inverter (NOT gate). The pull-down transistor has channel length and width of 15 and 500 μm, respectively; the pull-up transistor has channel length and width of 400 and 50 μm, respectively. The aspect ratios (Z) of the pull-up and pull-down are, then, 8.0 and 0.030, respectively. The geometric ratio (K_R), defined as $Z_{Pull\text{-}up}/Z_{Pull\text{-}down}$, is ~266. From the voltage transfer curve (VTC) of the inverter shown in Fig. 4(b), several voltages are defined, namely V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, V_{MAX}, and V_{MIN}. V_{OH} and V_{OL}, by definition, represent the minimum output voltage for a valid "1," and the maximum output voltage for a valid "0," respectively. The device dimensions were selected based on design studies using PSPICE to make V_{OL} close to 0 V and V_{OH} close to 2 V. V_{IL} (voltage input low) and V_{IH} (voltage input high) are the input voltages at which the output voltage transfer curve has the slope of 1.0. V_M (voltage midpoint) is the voltage where the input and the output voltages are equal. V_{MAX} (maximum output voltage) and V_{MIN} (minimum output voltage) are the maximum and minimum voltages that the output can reach. For the logic gate shown here, V_{OH}, V_{OL}, V_{IL}, V_{IH}, V_M, V_{MAX}, and V_{MIN} are 1.95, 0.45, 0.54, 1.03, 0.84, 2, and 0.22 V, respectively. The resulting noise margins, NM_L and NM_H, thus become 0.09 and 0.92 V, respectively. NAND and NOR logic gates can be realized simply by adding a transistor to the input node of the inverter in series configuration for the NAND gate and in parallel configuration for the NOR gate. Figure 4(c) shows output characteristics of NAND and NOR gates, respectively. V_A and V_B are the input voltages. For the NAND gate, the output becomes "0" only when both inputs are "1." For the NOR gate, the output becomes "1" only when both inputs are "0." The logic "0" and "1" outputs of the NAND gate were 0.03 and 1.98 V to 2 V, respectively. The logic "0" and "1" outputs of the NOR gate were 0–0.07 and 0.98–1.07 V, respectively. Collectively, these results and those of the individual transistors demonstrate that the combination of single-crystalline silicon nanomembranes and SANDs provides an important route to mechanically flexible, high performance, and low-voltage digital ICs on plastic substrates.

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