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Defect Tolerance and Nanomechanics in Transistors that Use Semiconductor Nanomaterials and Ultrathin Dielectrics**

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This paper describes experimental and theoretical studies of the mechanics of free-standing nanoribbons and membranes of single-crystalline silicon transfer printed onto patterned dielectric layers. The results show that analytical descriptions of the mechanics agree well with experimental data, and they explicitly reveal how the geometry of dielectric layers (i.e., the width and depth of the features of relief) and the silicon (i.e., the thickness and widths of the ribbons) affect mechanical bowing (i.e., ''sagging'') in the suspended regions of the silicon. This system is of practical importance in the use of semiconductor nanomaterials for electronic devices, because incomplete sagging near defects in gate dielectrics provides a level of robustness against electrical shorting in those regions which exceeds that associated with conventional deposition techniques for thin films. Field effect transistors formed using silicon nanoribbons transferred onto a range of ultrathin gate dielectrics, including patterned epoxy, organic self-assembled monolayers, and HfO_2, demonstrate these concepts.

1. Introduction

Interest in flexible, large area electronics and circuits for applications in consumer electronics, sensors, and medical devices has experienced recent and rapid growth.[1–4] As a materials approach to these kinds of systems, we have developed a technology to generate micro- and nanoscale objects of single-crystalline inorganic semiconductors using conventional microfabrication techniques with bulk or layered wafer substrates. In the case of silicon, micro/nanoribbons can be prepared from standard silicon-on-insulator (SOI) or bulk silicon (111) wafers by lithography and etching processes.[5,6] In this class of material, which we refer to as microstructured silicon (μs-Si), the typical thicknesses are between 50 and 500 nm, resulting in excellent mechanical bendability and the ability to integrate with nontraditional device substrates, such as thin plastic sheets for flexible electronics. Other similar elements can be formed from GaAs, GaN, InP using conceptually related ''top–down'' approaches.[7,8] For the purpose of device integration, we use a dry transfer printing technique to relocate the semiconducting objects from the mother wafer to a target substrate, where an element of a soft elastomer such as poly(dimethylsiloxane) (PDMS) provides the stamp.[9] With this materials and integration strategy, it is possible to create electronics on unusual substrates (e.g., plastic sheets, plates of glass) in two or three dimensional heterogeneous layouts, with device and circuit performance approaching that of conventional wafer-based technologies.[10–12] Related methods to similar systems,[13,14] as well as strategies that involve printing of solution suspensions of wires, rods, and other solid structures[15–17] are also of interest.

A unique feature of all of these types of approaches is that the key materials are delivered to the target substrate in the form of solid objects. This procedure is much different than conventional thin film strategies where the deposition process involves vapor or fluid transport of atomic or molecular species to the substrate. These differences are of both fundamental and practical importance. For example, small solid objects can span gaps and defects in the substrate, forming bridging structures that thereby reduce the sensitivity to surface roughness and thin film pinhole defects. This paper explores the relevant physics of this type of mechanics, through comprehensive experiment and theory. In particular, it studies the mechanics of bowing, or ''sagging,'' in μs-Si ribbons that span trenches and gaps on patterned dielectric structures. Examples of the utility of this mechanics are illustrated through the fabrication of high performance field effect transistor devices that use

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ultrathin gate dielectrics, with high levels of naturally occurring and engineered structural defects.

2. Results and Discussion

Figure 1a shows schematic illustrations of structures of μs-Si ribbons printed on layers of epoxy with lithographically defined trenches where the epoxy was completely removed. The ribbons can mechanically bow or "sag" in the regions of the trenches due to external loads such as gravity, or due to generalized adhesion forces such as electrostatic force and Van der Waals interactions between the ribbons and the underlying substrate. Electrostatics are most important when there is a significant difference in potential between the ribbons and the substrate.[18] Our AFM measurement conditions involve electrically grounding this system to minimize these effects, although we cannot rule out their role. Such sagging phenomena depend on the thickness of the epoxy (H), the width of the trench (W), and the thickness (t) of the μs-Si ribbons, as illustrated in Figure 1a. For example, the ability of the ribbons to bridge the trench without complete sagging increases with the thickness of epoxy. Figure 1a and b show, as examples, cases of complete sagging (Fig. 1a; $H = 54$ nm; $W = 10$ μm; $t = 100$ nm) and negligible sagging (Fig. 1b; $H = 749$ nm; $W = 10$ μm; $t = 100$ nm), which correspond to $H_{sag} = H$ and $H_{sag} = 0$, respectively.

To evaluate the physics of this sagging process and its origins, we printed μs-Si ribbons on patterned epoxy lines with different heights and line widths. Figure 2a shows AFM images patterns of epoxy with $H = 54$ nm height, and $W = 10$ μm (in line and space patterns, where the widths of the epoxy regions

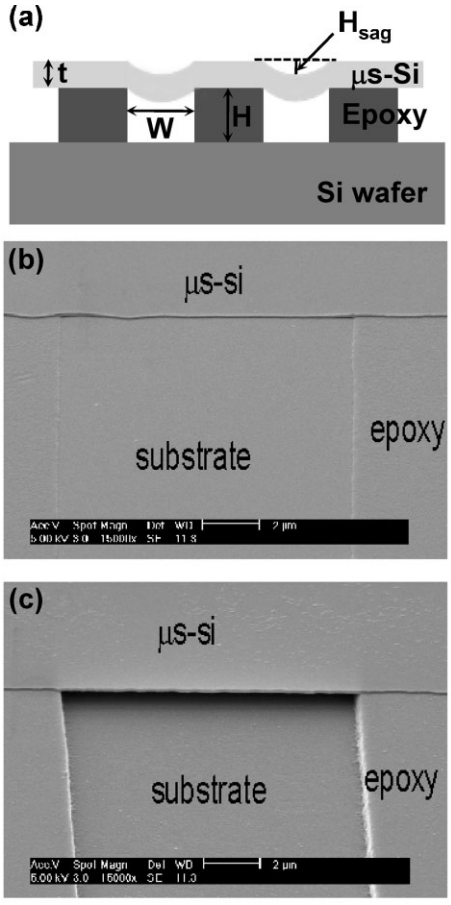

Figure 1. Thin ribbons of silicon printed onto patterned layers of epoxy. a) Cross-sectional schematic illustration, with definitions of key variables. b) and c) Scanning electron micrographs of ribbons of silicon completely collapsed (i.e., sagged) b) and perfectly suspended c) across a lithographically defined trench in a layer of epoxy with thickness of 54 and 749 nm, respectively.

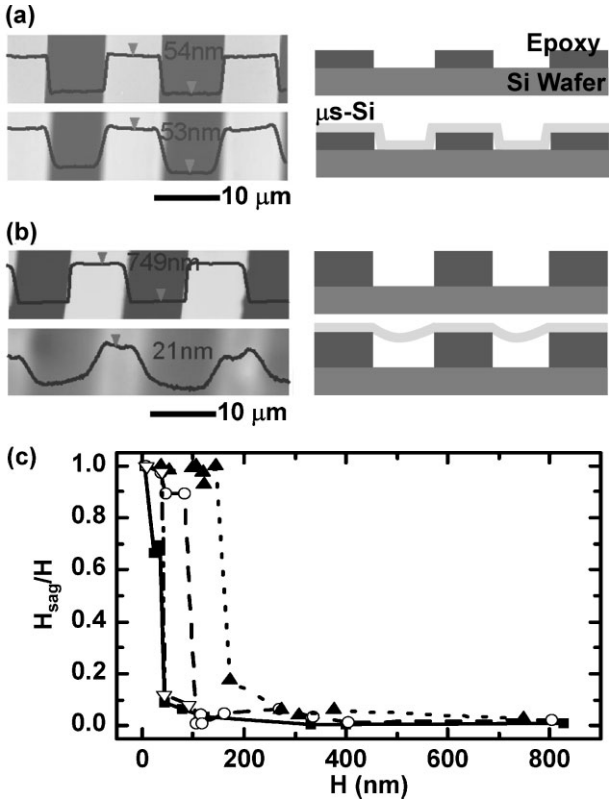

Figure 2. Sagging of thin ribbons of silicon on patterned lines of epoxy lines with different heights and spacings. a) Atomic force micrographs of a patterned layer of epoxy (top; thickness, $H = 54$ nm) and a similar structure with a 100 nm thick layer of silicon printed on top (bottom). The cartoon illustrations show these two different cases (right). These data indicate that the silicon is in a completely sagged state in the regions of the trenches. b) Atomic force micrographs of a patterned layer of epoxy (top; thickness, $H = 749$ nm) and a similar structure with a 100 nm thick layer of silicon printed on top (bottom). The cartoon illustrations show these two different cases (right). These data indicate that the silicon is in a nearly perfectly suspended state in the regions of the trenches. c) Plot of H_{sag}/H as a function of H for different trench widths (W), where the widths are equal to the spacing between the trenches. Filled squares: $W = 2$ μm; open circles: $W = 5$ μm; filled up-triangle: $W = 10$ μm wide. Open down-triangle: $W = 10$ μm wide. For all cases, the thickness of the silicon is 100 nm, except for the open down-triangles, which correspond to a silicon thickness of 290 nm.

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were equal to their spacings), before and after printing μs-Si ribbons with thicknesses of 100 nm. Linecuts through the AFM images show surface profiles with height variations of 54 and 53 nm before and after printing, respectively, indicating that the ribbons sag completely down to substrate, corresponding to $H_{sag} = H$. We believe that the sagging occurs immediately after printing. We used negligibly small applied pressures during printing to minimize mechanical strains that could cause sagging. By contrast, the surface profiles for μs-Si ribbons on epoxy with $H = 749$ nm, with otherwise similar W and layouts, $H_{sag} = 21$ nm, indicating that the ribbons are substantially suspended over the trenches (Fig. 2b). Figure 2c presents the ratio of H_{sag} to H as a function of H for W ranging from 2 to 10 μm. This ratio approaches 1 for the case of complete sagging and 0 for perfect suspension. As W increases, the ribbons undergo complete sagging on structures with progressively larger values of H. Of particular note is the abruptness of the transition between complete sagging and perfect suspension. This behavior is reminiscent of the snap-down characteristics observed in microelectromechanical devices.[19] For example, ribbons with $t = 100$ nm sag at $H = 10$ nm and $W = 2$ μm, and at $H = 84$ nm and $W = 5$ μm, respectively (Fig. 2c). In addition, thick Si ribbons of $t = 290$ nm tend to sag at lower H than thin ribbons of $t = 100$ nm.

The physics can be understood through analytical treatments of the mechanics. Figure 3 illustrates the geometry of the system that was analyzed. The function $w(x)$ describes the profile sagging (i.e., $w(x)$ is zero at $x = 0$ and is H at $x = c$). The maximum value of $w(x)$ is equal to the previously defined quantity H_{sag}. The total energy, U_{total} for displacement (i.e., sagging) of the suspended ribbon is related to the deformation energy and the adhesion energy by

$$U_{total} = U_{deformation} - U_{adhesion} \quad (1)$$

We assume here that the influence of gravity is negligible.[20] The validity of this assumption is examined at the end of the analysis. In Eq. (1), the deformation energy, $U_{deformation}$ and the adhesion energy, $U_{adhesion}$ can be obtained from the bending rigidity, $\overline{E}_{Si}I_{Si}$ [$\overline{E}_{Si} = E_{Si}/(1-\nu_{Si}^2)$, E_{Si} and ν_{Si} the Young's modulus and Poisson's ratio of Si, $I_{Si} = t^3/12$, and t is the thickness] as $U_{deformation} = \int_0^c \frac{1}{2}\overline{E}_{Si}I_{Si}[w(x)'']^2 dx$ and from the adhesion energy per unit area, γ between μs-Si and substrate as $U_{adhesion} = (a-c)\gamma$, respectively. If U_{total} at ground state is considered as zero, ribbon starts sagging when U_{total} is less than zero.

$$U_{total} = \int_0^c \frac{1}{2}\overline{E}_{Si}I_{Si}[w(x)'']^2 dx - (a-c)\gamma \leq 0 \quad (2)$$

Minimization of total energy $\partial U_{total}/\partial c = 0$ with respect to unsagged length, c gives

$$c = \left(\frac{3\overline{E}_{Si}t^3H^2}{2\gamma}\right)^{\frac{1}{4}} \quad (3)$$

We can fit the experimental data to determine the adhesion energy, γ, using this equation. Figure 4a shows the unsagged length, c as a function of H for $W = 10$ μm and $t = 100$ nm to fit the adhesion energy, γ per unit area between Si and μs-Si. The

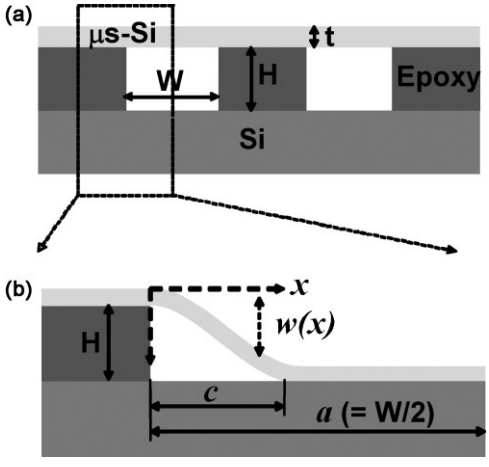

Figure 3. Schematic diagrams that define key variables for the theoretical analysis.

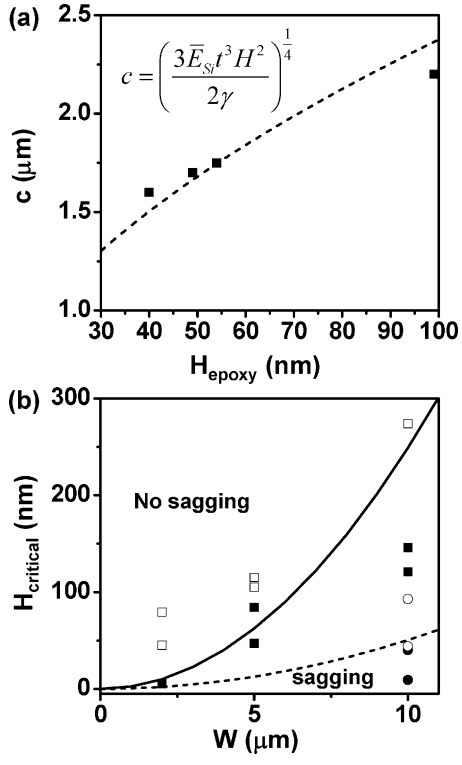

Figure 4. a) The unsagged length, c as a function of H for $W = 10$ μm and 100 nm thick Si ribbons measured experimentally (squares) and calculated theoretically where the adhesion energy (γ) per unit area was used as a single fitting parameter. b) Comparison of critical sagging height calculated from theoretical models with experimental results. The solid and dotted lines denote calculation results for 100 and 290 nm Si ribbons, respectively. The squares and the circles denote experimental results for 100 and 290 nm Si ribbons, respectively; open (suspending) and filled (sagging).

squares and the line denote measured data and result fitted from Eq. (3), respectively. For $E_{si} = 130$ GPa and Poisson's ratio, $\nu_{si} = 0.27$, γ is 66 mJ m^{-2}, which is comparable to literature values.[21]

There exists a critical thickness of epoxy, $H_{critical}$ at which the deformation energy and the adhesion energy are equal (i.e., the starting point of $H_{sag}/H = 1$), which is given by

$$H_{critical} = \frac{3\sqrt{6}}{64} W \sqrt{\frac{\gamma W^2}{\overline{E}_{Si} t^3}} \quad (4)$$

This equation predicts that $H_{critical}$ is proportional to the square of W. We can estimate $H_{critical}$ as a function of W using γ obtained from Figure 4a and Eq. (4) as shown in Figure 4b. For comparison of calculated to experimental results, we plotted the stable sagged and suspended configurations because it is difficult to define directly the critical point in experiment. The solid and dotted lines denote results calculated for 100 and 290 nm thick μs-Si ribbons, respectively. The solid squares and circles denote the stable sagged configurations from experimental results for 100 and 290 nm μs-Si ribbons, respectively, and the open squares and circles denote the suspended configurations. It is seen that the sagged and suspended regions agree well with predicted values. In the actual system, the sagging mechanics can be affected by factors such as environmental conditions, surface roughness, and surface treatment.[18,21] For example, a hydrophobic Si substrate coated with organosilane can exhibit lower adhesion. The surface roughness can also decrease the adhesion.[22]

The ability of the μs-Si ribbons to span gaps, trenches, and pinholes creates opportunities for building transistor devices that are extremely tolerant to structural defects in gate dielectric layers, of the type that would cause catastrophic failure in conventional thin film devices. To illustrate this capability, we built transistors using printed Si ribbons on epoxy dielectrics with intentionally patterned pinhole ''defects.'' Figure 5a shows a schematic illustration of a device structure and patterned dielectric. In devices that we examined, the channel lengths and widths were 7 and 100 μm, respectively. The silicon and epoxy thicknesses were 100 and 25 nm, respectively. A sheet of PET coated with ITO provided the substrate and the gate electrode.

The 25 nm thick layers of epoxy formed in the manner used here show large leakage currents, as illustrated by the filled squares in Figure 5b, which corresponds to current that flows between a film of Au (thickness = 100 nm, width = 100 μm) evaporated directly onto the epoxy and the underlying ITO. This behavior contrasts with the case for currents measured through similar structures, but with the Au layer replaced with transfer printed layer of Si with doped contacts ($t = 100$ nm, width = 100 μm, channel = 7 μm) where the gate leakage current is close to the noise limits in our setups (i.e., ~0.1 nA). This result indicates that the Si can span not only lithographically defined trenches but also those intrinsic to spin cast films.

Figure 5c shows an AFM image of a region of a dielectric intentionally patterned with defects in the form of circular

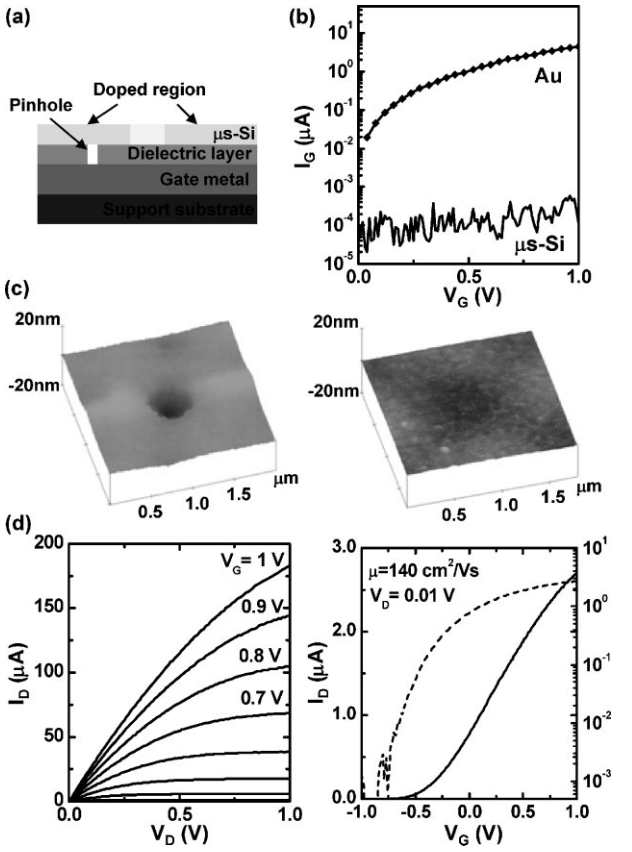

Figure 5. a) Schematic cross-sectional view of device structures of transfer-printed μs-Si on ultrathin dielectric layers. The pinhole represents an idealized view of a type of structural defect that can occur naturally or that can be introduced for the purpose of demonstration. b) Comparison of leakage currents measured in capacitor structures that consist of Au (top) and printed, Si (bottom) with doped contact on a 25 nm thick layer of epoxy dielectric film on an ITO (100 nm)/PET (180 μm) substrate. The ability of the Si to suspend over pinhole defects contributes to dramatically lower leakage compared to evaporated Au. c) Atomic force micrographs of a thin epoxy dielectric with a lithographically defined hole through its thickness before (left) and after (right) transfer printing of a layer of Si ($t = 100$ nm) on top. d) Electrical characteristics of a transistor with channel length and width of 7 and 100 μm, respectively: typical current–voltage characteristics (left) and linear and log scale plots of transfer curves collected at $V_D = 0.01$ V (right).

holes with diameters of 1 μm that extend completely through the thickness of the epoxy to the underlying ITO. This image shows that the silicon is perfectly suspended over this hole, thereby avoiding electrical shorting to the ITO. Figure 5d shows electrical characteristics of an μs-Si transistor having this design. The effective device mobilities, calculated using standard models,[23] are ~140 cm^2 V^{-1} s^{-1} in the linear regimes. The on/off ratio is ~10^4, with a threshold voltage of ~−0.3 V.

To illustrate the extreme level of insensitivity to pinhole type defects, we fabricated transistors on self-assembled monolayers (SAMs) and ultrathin, high-k metal oxide dielectric layers. Figure 6a shows, for example, electrical measurements on a device with $t = 100$ nm, channel = 7 μm, and width = 100 μm that uses a trichlorododecylsilane (TDS)

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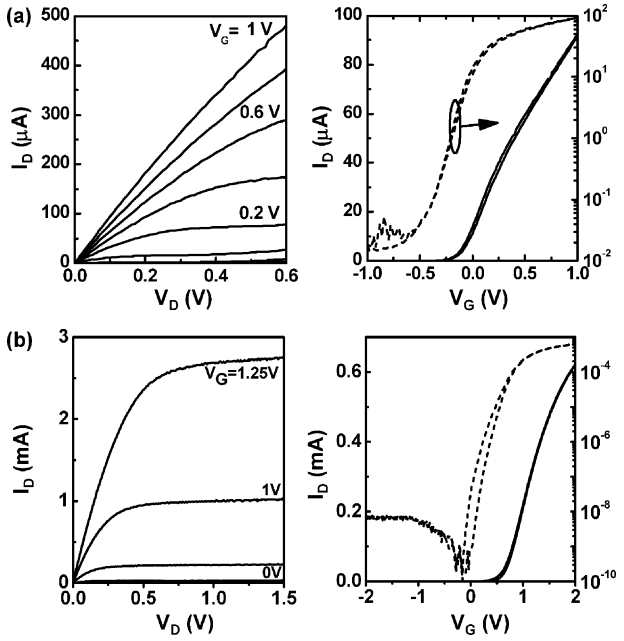

Figure 6. a) Electrical characteristics of a transistor that uses a SAM (thickness = 1.9 nm) as a gate dielectric, with channel = 7 μm and width = 100 μm: typical current–voltage characteristics (left) and linear and log scale plots of transfer curves collected at $V_D = 0.01$ V (right). b) Electrical characteristics of a transistor that uses a 4.7 nm thick layer of HfO_2 as a gate dielectric, with channel = 5 μm and width = 180 μm: typical current–voltage characteristics (left) and linear and log scale plots of transfer curves collected at $V_D = 0.05$ V (right).

SAM (thickness ~ 1.9 nm) on the native oxide of a doped silicon wafer. The effective device mobilities are ~120 $cm^2 V^{-1} s^{-1}$ in the linear regimes. The threshold voltage is −0.1 V, the on/off ratio is ~10^4, gate leakage is ~20 nA. The subthreshold slope is 150 mV $decade^{-1}$. Figure 6b shows representative current–voltage and transfer characteristics of a device with a channel length of 5 μm, and channel width of 180 μm that use ultrathin films of HfO_2 (thickness ~ 4.7 nm) formed on a silicon wafer. The effective device mobilities are ~140 $cm^2 V^{-1} s^{-1}$ in the linear. The on/off ratio is ~10^5, with a threshold voltage of ~0.6 V, the subthreshold slope is 100 mV $decade^{-1}$ and the gate leakage is ~8 nA. The mobilities of these devices are slightly lower than those of devices with SiO_2 dielectrics. This behavior may result from the relatively low quality of the interfaces.[24]

3. Conclusions

This paper describes essential aspects of the mechanics of classes of electronic devices that use solid, printed material nanostructures as components. The results reveal the physics associated with mechanical deformations that can cause these elements to conform to topographical features on the target substrate. As a practical matter, this type of mechanics has the advantage that it reduces greatly the sensitivity of such devices to roughness and other structural imperfections in the substrate or the layers that it supports. The same basic conclusions should also be applicable to other different, but related, types of device strategies that incorporate preformed wires, ribbons, tubes, rods, sheets, and other solid materials.

4. Experimental

Fabrication of Si Ribbons and Transfer Printing: Figure 7 shows the schematic illustration of steps for creating and then printing μs-Si ribbons with a stamp of PDMS. The fabrication begins with definition of thin ribbons of single-crystal silicon from an SOI (Soitec unibond with 100 or 290 nm top Si layer with doping level of $6.0 \sim 9.4 \times 10^{14}$ cm^{-3}) wafer. For transistor fabrication, the first step involved phosphorus doping, using a spin-on-dopant (Filmtronics, P509) and a photolithographically defined layer of SiO_2 deposited by plasma enhanced chemical vapor as a doping mask. After the doping steps, SF_6 plasma etching through a patterned layer of photoresist defined the μs-Si ribbons as a part of an interconnected mesh. Undercut etching of the buried oxide with concentrated HF solution (49% in water) released the μs-Si from the wafer. In the next step, contacting a flat elastomeric stamp of PDMS with the interconnected μs-Si ribbons and then peeling back the stamp removed the ribbons from the wafer and left them adhered, by van der Waals forces, to the surface of the stamp (Fig. 7a and b). Contacting the stamp, which now supports the interconnected μs-Si ribbons, to a substrate with a layer of dielectrics and then removing the stamp constituted the printing step (Fig. 7c). After the transfer-printing steps, SF_6 plasma etching through a patterned layer of photoresist defined the isolated μs-Si ribbons (Fig. 7d). These processes yielded arrays of μs-Si ribbons with various dimensions on different substrates, where they were then studied using various techniques as described in the following.

Fabrication of Mechanical Test Structures: Photolithographic techniques were used to pattern lines of epoxy, forming trenches in between, with desired geometries (line widths: 2 ~ 10 μm, lengths: ~1 cm, and spacings equal to their widths). The process began with spin-casting a precursor (Microchem SU8 diluted with 1 ~ 30% of SU8-2000 thinner) on Si wafer at 1500 ~ 5000 rpm, prebaking it at 65 and 100 °C for 1 min each, followed by exposing it to UV light for 10 s

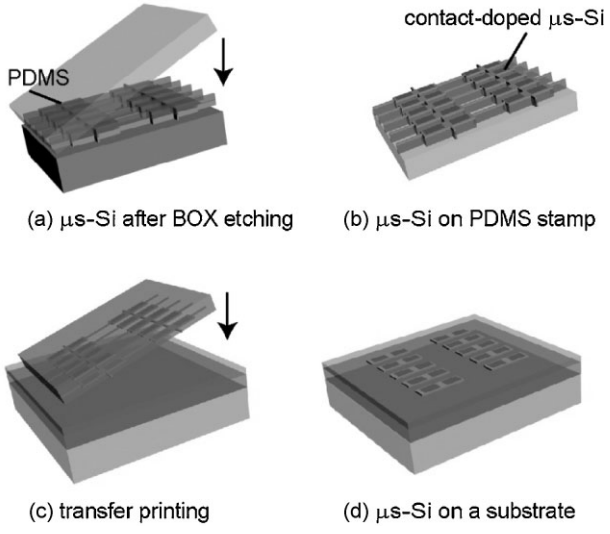

Figure 7. Schematic illustration of steps for fabricating and transfer printing interconnected, ultrathin ribbons (i.e., μs-Si) from a SOI wafer to a substrate.

through a photomask. After post-baking at 110 °C for 1 min, the unexposed epoxy was removed with SU8 developer, and then cured at 110 °C for 10 min. The epoxy had thicknesses between 5 and 800 nm. The surface profiles were measured using AFM (DI-3100, Veeco). The test structures were electrically grounded to eliminate electrostatic forces due to charges.

Fabrication of Field Effect Transistor Devices: The devices used bottom gate geometries in which the printed silicon ribbons provided the semiconductor, with dielectric films cast on gate electrodes on the target substrate. Metal electrodes patterned on the silicon provided the source and drain electrodes. Certain experiments used dielectrics with lithographically defined ''defects'' in the form of circular holes (thickness: 25 nm and hole size: 1 μm diameter) defined using procedures described in previous section. Monolayer dielectrics consisted of TDS (Sigma–Aldrich) SAMs formed by vapor deposition on a layer of oxide on a doped silicon wafer. The thicknesses were 1.9 nm, not including the ~1.4 nm of underlying oxide [25]. High-κ dielectrics based on HfO_2 were deposited on p-type silicon (100) substrates using a commercial atomic layer deposition (ALD) reactor (Savannah 100, Cambridge Nanotech.) and $Hf(NMe_2)_4$ precursors at a temperature of 250 °C. Before deposition, the substrates were etched in HF to remove the native oxide, and then rinsed in deionized water. The total thickness of the HfO_2 was ~4.7 nm. The capacitance (3.1 ± 0.2 μF cm^{-2}) was evaluated using by Agilent 4288A capacitance meter.

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