Complementary metal oxide silicon integrated circuits incorporating monolithically integrated stretchable wavy interconnects

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Stretchable complementary metal oxide silicon circuits consisting of ultrathin active devices mechanically and electrically connected by narrow metal lines and polymer bridging structures are presented. This layout—together with designs that locate the neutral mechanical plane near the critical circuit layers—yields strain independent electrical performance and realistic paths to circuit integration. A typical implementation reduces the strain in the silicon to less than ~0.04% for applied strains of ~10%. Mechanical and electrical modeling and experimental characterization reveal the underlying physics of these systems. © *2008 American Institute of Physics*.
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Stretchable electronics is emerging as a technology that could be valuable for various applications, such as conformal personal or structural health monitors and hemispherical detector arrays. Such devices cannot be accomplished with conventional wafer based circuits. Presently, the following two approaches exist for achieving stretchability: one uses rigid device islands interconnected by separately fabricated stretchable interconnects,[1] another exploits fully stretchable integrated circuit systems.[2] A disadvantage of the former is that large scale integration can be difficult, due to the nature of the fabrication procedures. The latter suffers from slight changes in device characteristics that can be induced by the strains associated with stretching. Here we present an approach that combines these two concepts, in a way that naturally incorporates the strengths of each. These systems consist of complete integrated circuits formed on ultrathin flexible plastic supports that are patterned in a manner that isolates interconnects and mechanical bridging structures. Bonding to a prestrained rubber substrate followed by relaxing of this prestrain leads to systems with monolithically integrated, stretchable "wavy" interconnects and bridges. Mechanical response to stretching involves, primarily, deformations only in these interconnects and bridges, thereby avoiding unwanted strains in the regions of the active devices. We demonstrate these concepts through comprehensive mechanical analysis and electrical characterization of stretchable complementary metal oxide silicon (CMOS) circuits based on single crystalline silicon.

Figure 1(a) shows a schematic illustration of the fabrication process, for CMOS inverters. The semiconductor consisted of doped nanoribbons of single crystalline silicon, transfer printed onto a carrier wafer coated with a bilayer of poly(methyl methacrylate) (PMMA) (MicroChem, USA) and polyimide (PI) (Sigma Aldrich, USA) having thicknesses of 100 nm and 1.2 μm. The CMOS inverters were fabricated by using procedures related to those reported recently.[2,3] Spin coating the resulting circuits with a PI layer (~1.2 μm) positioned the circuit layers near the neutral mechanical plane of the composite structure. Next, reactive ion etching through patterned etch masks removed regions of the PI encapsulant, substrate, and underlying PMMA layer, to isolate the interconnects, to define structural bridges and to create a periodic array of circular openings. These openings facilitated the dissolution of the PMMA with acetone, to release "segmented" ultrathin circuits. Depositing Cr/SiO_2 (330 nm) onto the backside of lifted-off circuits enabled covalent bonding to a piece of prestrained polydimethylsiloxane (PDMS) (Dow Corning, USA). Thermal expansion of the PDMS (to 160 °C) provided biaxial prestrains of ~3.9%. Releasing the prestrain induced the wavy structures in the narrow interconnects and structural bridges, as shown in sec-

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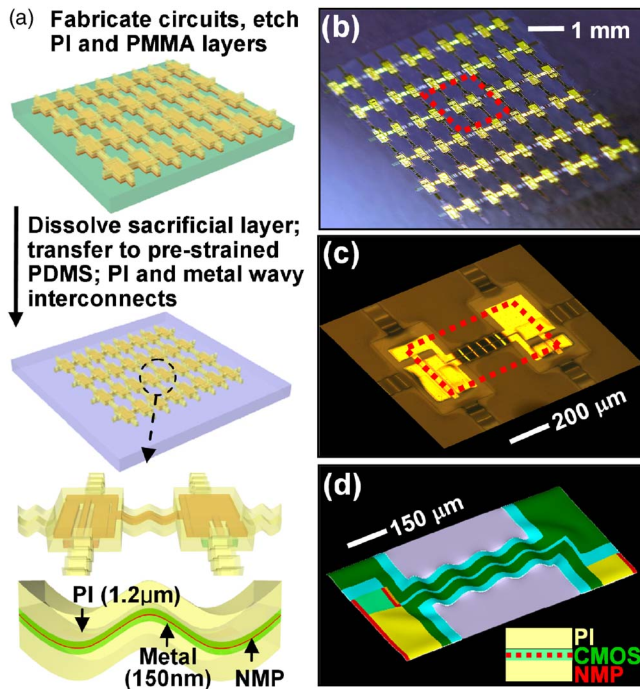

FIG. 1. (Color online) (a) Schematic illustration of the fabrication process, including cartoons of CMOS inverter logic gates with stretchable, wavy interconnects. Also shown is the strategy of top layer encapsulation to locate the critical circuit elements near the neutral mechanical plane (NMP) to avoid cracking. (b) Image of CMOS inverters with wavy interconnects and bridge structures. (c) Magnified view of a CMOS inverter with wavy interconnects. (d) Three dimensional finite element simulation of the mechanics of this system, showing good agreement with experimental observation; inset shows the location of neutral mechanical plane at the active island region.

ond frame of Figs. 1(a) and 1(b). The "island" regions containing the active devices remained largely unperturbed. Figure 1(c) provides a magnified view of this type of wavy CMOS inverter, which shows clearly the flat island region with wavy metal and PI interconnects. The low strain at the island region can be confirmed through full three dimensional finite element modeling, as shown in Fig. 1(d). In addition, the top layer of PI provides a neutral mechanical plane design to help avoid cracking for both the Si active region (where strain minimization is also important to reduce stretching/bending induced changes in the electronic properties) and the metal interconnect, as schematically shown in the inset of Fig. 1(d) and bottom frame of Fig. 1(a), respectively. The simulations were performed using the nonlinear finite element analysis package ABAQUS (Ref. 4) to follow the same fabrication steps as in the experiments. Even though this array design and neutral mechanical plane layout reduce the probability of failure by fracture, it is possible that extended cycling to levels of stretching that cause significant strain in the metal could lead to failures via well known mechanisms such as stress voiding, creep and others.[5] Cycling tests of 30 times on related devices by two dimensional thermal stretching up to ~3.9% and releasing showed minimal changes (<~15% in electrical properties).[2] Other more recent tests show little degradation for >1000 cycles.

We performed stretching tests on these inverters, in both the x and y directions [Fig. 2(a)]. Due to the ability of the wavy interconnects to absorb applied strains, the islands do not show significant deformations even for local strains of 3.7%. Behaviors consistent with the Poisson effect can also

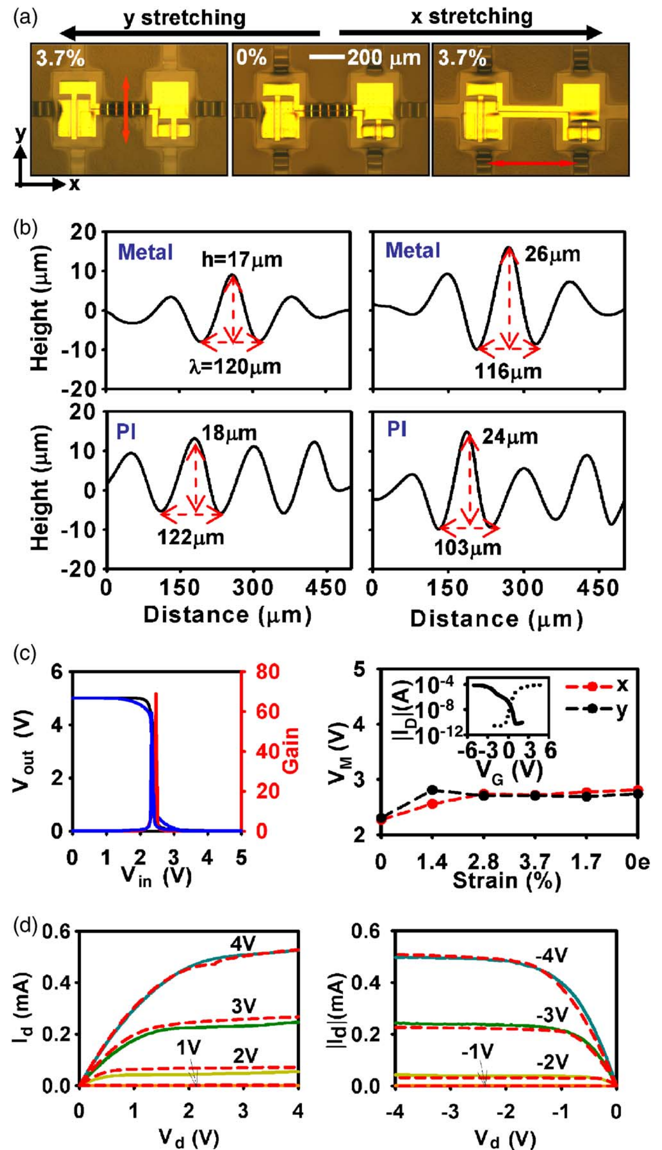

FIG. 2. (Color online) (a) Optical images of stretching tests on a silicon CMOS inverter. (b) Profile changes associated with the Poisson effect with applied strain of 3.7% along y (left) and x (right). (c) Transfer characteristics of stretchable CMOS inverters (red and black: experiment, blue: simulation, left) and variation in inverter threshold voltage for each applied strain in x (red) and y (black) direction (right); the inset shows log scale transfer curves for individual transistors. (d) Current-voltage curves of an nMOS (left) and pMOS (right) transistor; solid and dotted lines correspond to experiment and simulation, respectively.

be observed in profiles of Fig. 2(b). In particular, when we stretch the PI bridge in the y direction, the metal bridge experiences compression (and vice versa), such that the wavelength decreased from 120 to 116 μm, while the amplitude increased from 17 to 26 μm, as shown in top two frames of Fig. 2(b). Also when the metal bridge is stretched in x direction, the PI bridge is compressed, thereby changing the wavelength of the PI bridges from 122 to 103 μm and amplitude from 18 to 24 μm, as shown in the bottom frames of Fig. 2(b). The electrical properties are consistent with this mechanics of deformation. In the as-fabricated state, without applied strain, the inverters showed expected transfer characteristics with gains as high as ~70, consistent with PSPICE simulation based on separate measurements of individual transistors [Fig. 2(c), left]. The mobilities were ~310 and

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~150 $cm^2/V\,s$ for *n*-type MOS (nMOS) and *p*-type MOS (pMOS) devices, with on/off ratios $>10^5$ for both types of devices [Fig. 2(c), inset]. For the CMOS inverters, the channel lengths and widths were 13 and 100 μm for nMOS and 13 and 300 μm for pMOS, respectively. Under various applied strains, the electrical properties showed little variation. For example, the inverter threshold voltage changed by less than ~0.5 V for strains between ~3.7% in *x* direction and ~3.7% in *y* direction, as shown in the right frame of Fig. 2(c). Also Fig 2(d) shows IV curves, in which solid lines are experimental results and dotted lines are simulation results obtained by PSPICE. These strain independent behaviors represent significant improvements over similar circuits that do not use isolated interconnect and bridge structures,[2] thereby validating the designs introduced here. Mechanics analysis is consistent with these observations. For the prestrain 3.9% in experiments, analysis based on energy minimization gives the wavelength 127 μm and amplitude 18.6 μm for the metal bridge, which agree well with experimental values 120 and 17 μm, respectively. The maximum strain in the Si layer is only 0.04%. Even for a much larger prestrain 10%, the maximum strains in the Si, metal and SiO_2 layers are 0.07%, 0.50%, and 0.73%, respectively, which are one third to one half of their counterparts without isolated interconnect and bridge structures.[2] This result occurs because the bridge structures buckle to accommodate the large prestrain, which protects the device islands from buckling and therefore reduces the strain. The major failure mode, therefore, is damage to the metal bridges. The top PI layer shifts the neutral mechanical plane in a way that reduces the strain in these critical bridge layers.

The inverters in Figs. 1 and 2 can also be stretched in any angle. The angled stretching is equivalent to stretching along the bridge directions *x* and *y* plus an in-plane shear. Since the thickness (~2.5 μm) is much less than the width (~100 μm), the large in-plane shear leads to "lateral buckling"[6] out of the plane such that the strains remain small. This mechanics is related to a mesh based approach by Someya *et al.*[7] In this case, rotation and bending of struts provide large degrees of stretchability in certain, but not all, directions. This approach is fully compatible with layouts and fabrication approaches presented here.

The stretegy of Fig. 1 can be applied not only to inverters, but also to more complex circuits. Figure 3 shows three stage CMOS ring oscillators and stretching tests in the *x* and *y* directions. The geometries of the transistors and the prestrain were the same as those for the inverters discussed previously. In this circuit, all nMOS and pMOS islands were interconnected with four horizontal and three vertical interconnects, and each ring oscillator was connected with structural bridges, as illustrated in Fig. 3. The oscillation frequency is ~2.3 MHz at a supply voltage of 10 V. The change in frequency with stretching is less than 0.3 MHz, up to strains of nearly 4% [Fig 3(b)]. As with the individual inverters, this level of strain independent performance represents an important improvement over previous results.

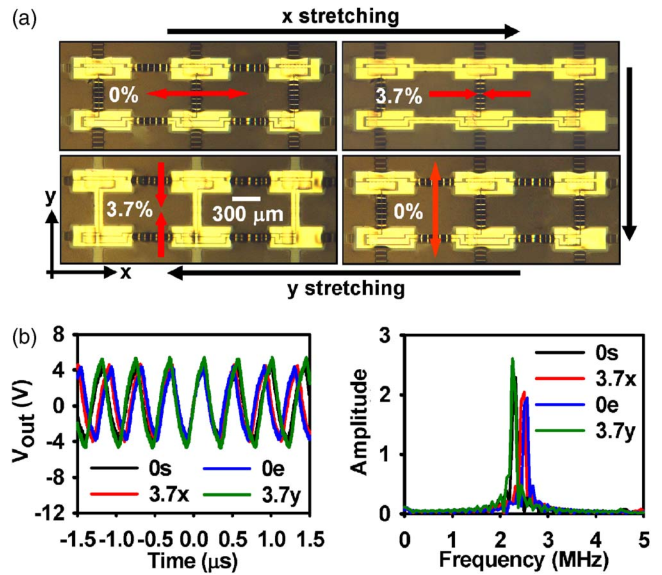

FIG. 3. (Color online) (a) Optical images of stretching tests on a silicon CMOS ring oscillator. (b) Oscillation characteristics at different strain values (left: 0s and 0e refer to zero strains at the start and end of the tests, respectively: 3.7*x* and 3.7*y* refer to 3.7% tensile strains along *x* and *y*, respectively) and associated frequencies determined by Fourier transformation (right).

In conclusion, by structuring the types of ultrathin substrates implemented in separately reported stretchable circuit designs, it is possible to localize mechanical deformations in noncritical regions to remove any measurable dependence of the electrical performance on applied strain. This design concept is validated by mechanics analysis and electrical measurements on representative circuits. Further development to increase the range of stretchability represents a topic of current work.

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