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Flexible Electronic Building Blocks

Semiconductor Wires and Ribbons for High-Performance Flexible Electronics

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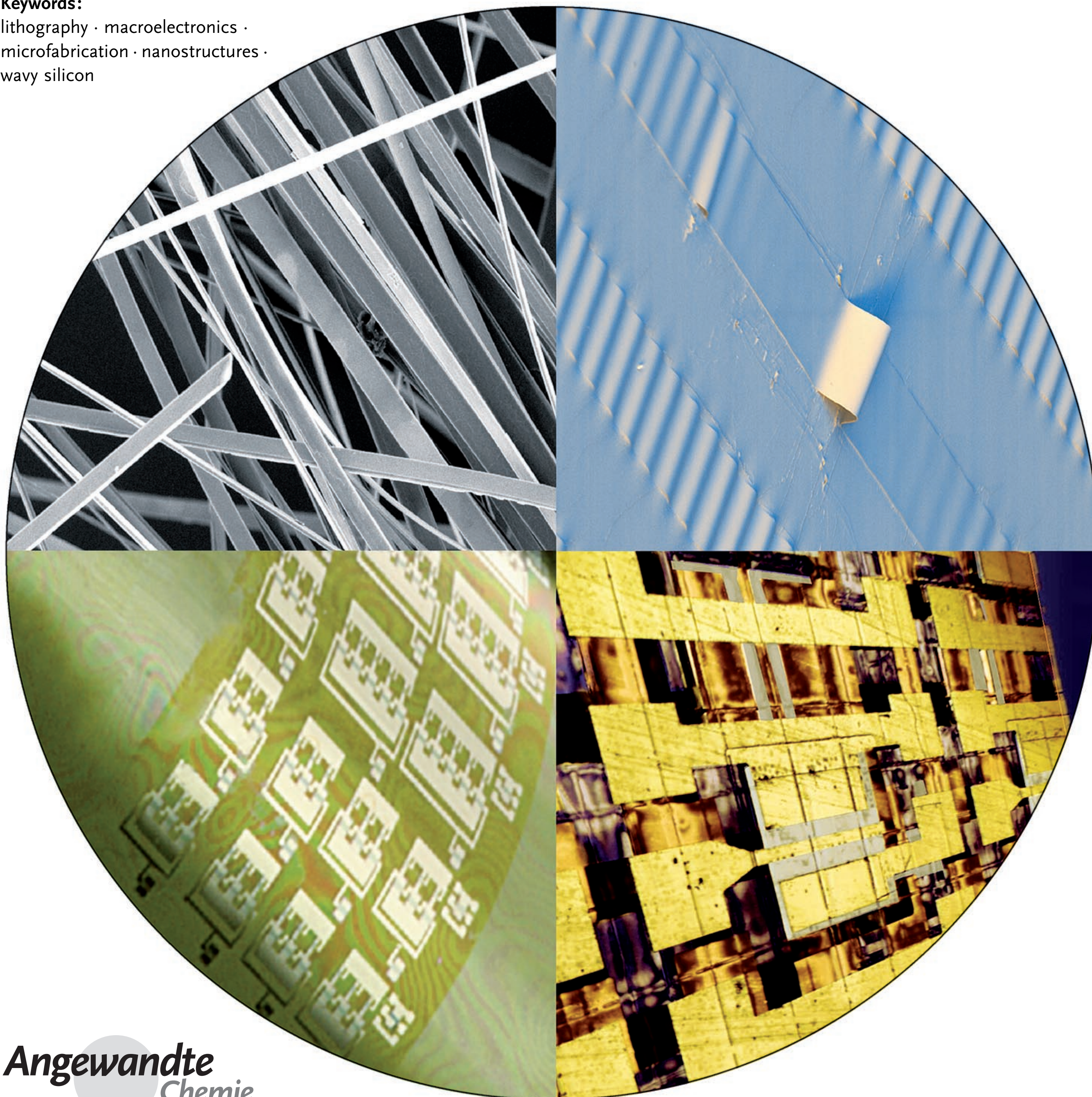

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This article reviews the properties, fabrication and assembly of inorganic semiconductor materials that can be used as active building blocks to form high-performance transistors and circuits for flexible and bendable large-area electronics. Obtaining high performance on low temperature polymeric substrates represents a technical challenge for macroelectronics. Therefore, the fabrication of high quality inorganic materials in the form of wires, ribbons, membranes, sheets, and bars formed by bottom-up and top-down approaches, and the assembly strategies used to deposit these thin films onto plastic substrates will be emphasized. Substantial progress has been made in creating inorganic semiconducting materials that are stretchable and bendable, and the description of the mechanics of these form factors will be presented, including circuits in three-dimensional layouts. Finally, future directions and promising areas of research will be described.

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1. Introduction

During the last half century, aggressive reductions in the critical dimensions (i.e. channel lengths and dielectric thicknesses) of transistors in microelectronic systems have led to enormous increases in speed, functionality, and computing capacity. This trend is likely to continue for some years, leading to devices and systems with exceptional operating characteristics. Over the last ten years, a much different class of electronics, sometimes referred to as "*macroelectronics*", has emerged to reach a cumulative economic significance, defined by market size, that is only a few times less than that of conventional microelectronics.[1–8] Progress in this relatively new field, in which circuits are distributed over substrates that are much larger than even the largest semiconductor wafers, is often measured by overall systems size, rather than the dimensions of individual elements in these systems.[9,10] The most prevalent examples of macroelectronic devices are flat-panel displays that use thin film transistor (TFT)-on-glass technology for active matrix pixel addressing. The commercial success of these displays could lead to new applications of macroelectronics, including digital X-ray imagers, flexible photovoltaic systems, paper-like displays, conformal structural health monitors, and others, in which lightweight, flexible substrates facilitate system transport and use.[9–18] These and other possibilities create substantial interest in materials and fabrication techniques that enable electronic devices to be formed, in scalable ways, directly on flexible substrates such as metal foils or, ideally for many end uses, thin sheets of plastic. The main challenge is that the characteristics of the substrates and the large-area requirements often impose limitations on materials choices and fabrication processes. For example, most low-cost polymer substrates degrade at temperatures above 300 °C, making them incompatible with conventional techniques for the deposition and doping of most established classes of inorganic semiconductors.

Small-molecule organic and polymer semiconductors represent types of materials that are attractive for these applications because of their good mechanical flexibility, low-temperature processibility, and inherent compatibility with plastics.[11,19,20] Transistors that incorporate these materials have been used for flexible and rigid displays based on light-

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emitting diodes,[21,22] electrophoretic inks,[11] polymer-dispersed liquid crystals,[23] and others,[24–26] as well as radio-frequency identification tags[27] and sensors.[28] The difficulty in obtaining high performance, as measured in terms of the device mobilities, restricts, however, the range of application possibilities. One means to avoid these limitations is to use, in place of the organic semiconductors, polycrystalline silicon formed by high power, pulsed ultraviolet laser recrystallization of thin films of amorphous silicon or solution processed thin silicon films.[29] Thermal barrier layers can isolate, to some extent, the laser heated silicon from underlying layers, thereby allowing such methods to be applied with certain classes of high-temperature plastic substrates (e.g. polyimide).[30] Although these approaches can yield transistors with impressive properties,[31–37] the procedures are complex and will require sophisticated setups to implement over large areas with suitable levels of uniformity. A different and more recent technique involves the incorporation of single-crystal inorganic semiconductors directly, in the form of separately synthesized micro- or nanoscale structures. These elements can be in the form of nanocrystallites,[38,39] although geometries that minimize barriers to charge transport that can form at the interface between elements, such as wires, ribbons, platelets, and related,[40–42] are preferred. These elements can be created either from the "bottom-up"[43–47] by vapor- or liquid-phase chemical synthesis or from the "top-down" by controlled etching of single-crystal wafers or thin film sources of material.[42,48–52]

This article reviews aspects of single-crystal inorganic semiconductor wires/ribbons formed by using both "bottom-up" and "top-down" procedures, and their integration into flexible electronic devices. The content begins, in Sections 2 and 3, with summaries of some considerations on the mechanical flexibility of these elements, and methods to create them. Sections 4 and 5 present strategies for integrating them into devices and circuits, together with some features of the electrical properties of these systems. Section 6 presents results of devices that offer not only mechanical flexibility but also full, reversible stretchability, and summarizes the current state of the field and presents some perspectives on trends for future work.

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2. Mechanics of Bending and Stretching

The implementation of micro- or nanoscale structural forms of inorganic semiconductor materials in flexible electronics relies critically on their ability to be bent repeatedly without fracture. These elements experience tensile and compressive strains when bent into convex or concave shapes, respectively. Typical inorganic semiconductors fracture at tensile strains in the range of 0.5–1.0%. Other failure mechanisms in circuits and devices on plastic include interfacial slippage or delamination associated with motions, relative to the substrate, in directions parallel or perpendicular to the substrate surface, respectively. The mechanics of these systems must, therefore, be understood to achieve reliable devices. We outline here some aspects of bending, and even stretching, of this class of electronic building block.

The dimensions and mechanical properties of the micro- or nanoscale semiconductor elements, in the form of wires, ribbons, bars, or membranes, determine their bending mechanics.[53] The planar layouts of these elements, as implemented in devices, and the comparatively high in-plane rigidity of the plastic substrates allow us to ignore deformations for which the lateral dimensions are important. Figure 1 A presents a schematic of a ribbon with thickness t

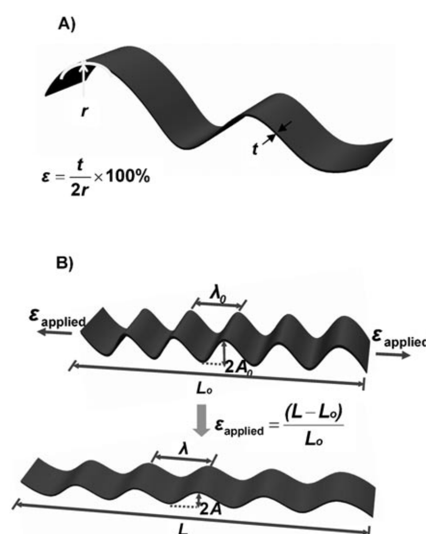

Figure 1. Schematic illustration of bendable (A) and stretchable (B) semiconductor objects. In most implementations, at least one of the dimensions (i.e. thickness, t) is in the nanometer or micrometer regime.

bent to a radius of curvature r. The top and bottom surfaces are under tensile and compressive strains, respectively. In the regime where t is small compared to r the peak strain is given by the simple expression in Equation (1):[54]

$$\varepsilon = \frac{t}{2r} \times 100\% \quad (1)$$

For silicon ribbons with $t \approx 0.1$ μm, tensile strains sufficient to crack the silicon (i.e. $\approx 0.7\%$) will occur only when r is

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less than about 7 μm. This degree of bending vastly exceeds the requirements for most envisioned applications, where $r \approx 1$ cm is often sufficient. In devices, however, the ribbons must reside on the top or bottom surface of a substrate such as a sheet of plastic. As a result, when the substrate is bent, the devices experience strains determined by Equation (1), with, approximately, a value of t that corresponds to the thickness of the substrate. A substrate with a thickness of 50 μm, which is typical for many contemplated applications, will have surface strains of 0.7% when bent to $r \approx 3.5$ mm, assuming that the semiconductor/substrate interface does not fail. A practical design rule might be that the silicon strain must remain below 0.1%, which leads to a degree of bendability of $r \approx 2.5$ cm for this type of substrate, which is still sufficient for many applications. The degree of bending can, of course, be improved simply by reducing the thickness of the substrate. For example, a substrate with thickness of 25 μm would enable a bend radius of about 1.25 cm for the system described above. Although this strategy can be useful, most practical applications benefit from some degree of flexural rigidity in the substrate. Alternative paths to increased bendability that avoid low rigidity and use relatively simple principles of mechanical engineering can be considered. For example, in a bent sheet, strains are compressive on one surface and tensile on the other, with an approximately linear variation between these two extremes. A zero crossing occurs at the midplane, commonly referred to as the neutral mechanical plane, within the limits of applicability of Equation (1).[55,56] Circuit elements can be located at this plane by, for example, fabricating devices on the surface of a plastic substrate and then, subsequently, laminating another sheet of plastic, with similar thickness and mechanical properties to the bottom substrate, on top.[55,56]

The key concept, then, is that thin substrates with thin semiconductor elements and/or neutral mechanical plane designs enable bendability. Stretchability is a different and much more challenging characteristic. Interest in stretchable electronics derives not only from the extreme levels of bendability that can be achieved, but also from the ability to integrate electronics with complex curvilinear surfaces, such as hemispheres for electronic eye imagers, wings of an aircraft for structural health monitoring, and biological systems for implants, sensors, or wearable electronics. None of these examples is possible with electronics that offer only bendability (flexibility); stretchability is required. One approach relies on thin devices[57–59] and interconnects[60,61] that are structured into "wavy" shapes. In this layout, the overall systems can be stretched reversibly to large levels of strain without fracturing the materials because these strains can be accommodated through changes in the amplitudes and wavelengths of the wavy structures.[57–61] Although detailed analysis is required to capture accurately the mechanics of such wavy structures, their qualitative behavior is entirely consistent with the physics of an accordion bellows, in which the wavelength (λ) and amplitude (A) vary with applied strain according to Equations(2) and (3).

$$\lambda \approx \lambda_0(1+\varepsilon_{\text{applied}}) \tag{2}$$

$$\lambda_0 = \int_0^{\lambda} \sqrt{1+\frac{4\pi^2 A^2}{\lambda^2}\sin^2\left(\frac{2\pi}{\lambda}x\right)}\,\mathrm{d}x \tag{3}$$

λ_0 is the wavelength in the unstrained configuration, A is the amplitude, and $\varepsilon_{\text{applied}}$ is the applied strain, for the case that $\varepsilon_{\text{applied}}$ is small compared to the strain needed to create the wavy geometry with wavelength λ_0 (Figure 1B).

3. Fabrication of Micro- and Nanoscale Semiconductor Elements

Generating semiconducting objects of the type needed to achieve these flexible or stretchable configurations from materials such as silicon, germanium, carbon, and III–V compounds such GaAs, InP, and GaN are of particular interest. The following sections summarize approaches based on "bottom-up" synthesis and "top-down" fabrication. Both have demonstrated promise for generating micro- and nanoscale semiconducting elements suitable for use as active building blocks in macroelectronic circuits.

3.1. Bottom-up Approaches

In the most general sense, synthetic methods for forming one- or two-dimensional single-crystalline semiconductor objects rely on the ability to condense and grow an assembly of semiconducting atoms by breaking the symmetry of their crystal lattices, a process which has been reviewed recently.[47,62] One of the most successful approaches is the vapor–liquid–solid (VLS) method, originally developed by Wagner and Ellis.[63] The VLS method relies on controlling the reaction conditions of a gaseous precursor with catalytic metal nanoparticles. Choices of the metal semiconductor compositions, metal catalysts, and reaction temperatures are dictated by examining the metal/semiconductor binary phase diagram of the materials of interest.[45,47] Monodisperse metal clusters are arranged onto a substrate, followed by the introduction of a gaseous semiconductor precursor. At a certain temperature, atoms of the semiconductor condense onto the surfaces of the metal nanoparticles. When the concentration of the semiconducting atoms supersaturates the catalyst, the metal nanoparticles melt, thereby forming liquid alloyed droplets. Further introduction of semiconductor precursor results in a nucleation process in which the solid semiconductor phase precipitates from the alloyed droplet. Well-aligned nanowire arrays can be fabricated in orientations normal to the substrate surface by epitaxial growth with patterned catalyst.[64–66] By combing these oriented growth mechanisms with patterned catalyst particles, it is possible to achieve control over the orientations, positions, and densities of the nanowire arrays. In a different strategy, placing catalyst particles on the surface of a nanowire,[67] or growing nanobars on quantum dots,[68] can lead to branched nanostructures.[67] For example, the formation of branched networks of lead selenide (PbSe) nanowires can be achieved by exposing the

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PbSe reactant to a vapor of a low melting point metal catalyst during the nanowire growth process.[69]

In addition to control over shape and position, the materials compositions can be modulated, either axially or radially, through the use of clever growth strategies. For example, nanowires can be formed with different materials in core–shell layouts by controlling the growth conditions such that the incoming vapors preferentially coat the nanowire surfaces.[70] Also, multishell nanostructures can be achieved by introducing reactants and dopants of varying compositions.[70] Similar heterostructures composed of metal and semiconductor materials have been recently fabricated by depositing Ni metal onto Si nanowires synthesized by VLS.[71] This process enables the integration of metal contacts (i.e. metal silicide formation), thereby facilitating the integration of these nanowires into electrical systems.

A technique related to VLS is known as the solution–liquid–solid (SLS) process. The synthesis in this case occurs in a liquid phase with low melting point metal nanoparticles as catalysts and with solvents with high boiling points.[72,73] The semiconductor atoms derive from organometallic precursors that decompose at high temperatures. The SLS process can generate nanowires of silicon[74,75] and other materials, including III–V compounds.[72,73] In one example, GaAs nanowires with diameters ranging from 10–150 nm follow from the alkane elimination reaction given in Equation (4).

$$t\mathrm{Bu_3M} + \mathrm{EH_3} \rightarrow \mathrm{ME} + 3\,t\mathrm{BuH} \quad (4)$$

M stands for an element of Group III, E stands for an element of Group V, and ME stands for the synthesized III–V nanowire. The use of (tri-*tert*-butyl)indane and -gallane in the presence of catalytic protic solvents generates III–V nanowires in yields of 50–100%. When implemented with indium nanoparticles as catalysts, this process yields nanowires with narrow diameter distributions (i.e. 14–16% variations), and dimensions down to about 6 nm.[73]

Another interesting approach that is conceptually different than either VLS or SLS, uses molecular nanostructures such as carbon nanotubes[76] and DNA molecules[77,78] as supporting elements or step edges in substrates such as highly oriented pyrolytic graphite (HOPG)[79–81] for the formation of wires of other materials, with dimensions as small as 3 nm.[78] For instance, metal nanowires composed of Au, Pd, Fe, Al, Pb,[82] MoGe,[83,84] and Nb[76] have been formed with nanotube supports. Interestingly, these nanowires can become crystalline when irradiated with electrons.[78] Similar structures can be formed by using DNA instead of nanotubes.[77,78] Metallic nanowires formed in this fashion are homogeneous and exhibit superconductive properties at low temperatures.[77,78] The ability of DNA molecules to self-assemble into complex structures suggests routes to organized arrays and other layouts of wires that might be useful for devices.

3.2. Top-down Approaches

Micro- or nanoscale structures, primarily nanowires, generated by bottom-up approaches have advantages that certain unusual heterostructures can be fabricated, large quantities of material can be formed, and very small dimensions can be achieved. The wires, however, are often relatively short ($\lesssim$ 100 μm),[45,47,72–74,85,86] and the characteristic sizes, particularly for ribbon geometries, have broad distributions.[87–100] Methods to control the surface properties, compositional purity, doping uniformity, and concentration are also much less well developed than those employed with wafers used by the semiconductor industry. As a result, these wafers, together with the processing approaches that have been developed to create high-performance, reliable devices from them, become attractive for potential use in an area like macroelectronics. The following section describes some strategies for forming micro- and nanoscale semiconductor elements from high quality single-crystal wafers and thin films by using top-down techniques. We refer to elements fabricated in this way, as microstructured semiconductors (μs-sc), such as microstructured silicon (μs-Si), microstructured gallium arsenide (μs-GaAs) and so on.

Lithographic processing and etching techniques can create these elements. In the simplest approach, layered wafers such as silicon on insulator (SOI), GaAs/AlAs/SiGaAs, or AlGaN/GaN/Si provide substrates that can be patterned with a resist and then etched to remove a sacrificial layer or underlying support (e.g. SiO_2 for SOI; AlAs for GaAs/AlAs/SIGaAs; Si for AlGaN/GaN/Si) thereby producing ribbons, wires, platelets, or bars.[42,49,51,58,59,101] The lithography processes, often based on conventional methods such as photolithography[42,51,102] and electron beam lithography,[103–105] or newer techniques such as soft lithography[51,106] and nanoimprint lithography,[107,108] define the geometries and spatial layouts of these elements. With proper control of the procedures, extremely smooth surfaces and excellent mechanical properties can be achieved,[42,51] with dimensions down to the 10 nm range in thickness,[42,51,108,109] and lateral dimensions down to 17 nm.[102,108,110]

The lateral dimensions of these structures can range from the very small (i.e. wires with dimensions down to $\approx$20 nm) to the very large (i.e. membranes with dimensions of several cm), and anything in between. Examples of small structures are formed by using a lithographic technique known as superlattice nanowire pattern transfer (SNAP).[101] In this approach, the etched edge of a superlattice consisting of GaAs/AlGaAs layers capped with a layer of evaporated metal is placed into contact with an adhesive coated substrate, such as an SOI wafer. Next, the metal layer is released from the superlattice structure by selectively etching the GaAs layer. The transferred metal layer on the SOI substrate serves as a mask for subsequent etching steps to define the nanowires.

Large, freestanding single-crystal sheets[109,111] and tubes[112–116] can also be created from wafers that employ an embedded release layer. For example, elastically strained SiGe nanomembranes can be fabricated on SOI wafers and transferred onto a variety of different substrates,[109] including polymer substrates for flexible electronic applications.[117,118] Moreover, nanotubes and other unusual structures can be fabricated by depositing layers of Ge, GaAs, and related compounds onto a host substrate (e.g. silicon) by molecular

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beam epitaxy.[113–115] In this case, the diameter of the tubes is defined by the layer thicknesses and built in strains.[113] Fabrication of micro- and nanostructures using wafers with an embedded sacrificial layer is attractive due to the versatility, and experimental simplicity of the approach. Disadvantages include costs that can be considerable for electronics that require large numbers of functional elements, and an absence of convenient means to create bulk quantities of material. As a result, routes for generating micro- and nanoelements from bulk wafers are of interest.

In one such approach, anisotropic chemical etching of III–V compound wafers with a (100) top surface and zinc blende face-centered cubic crystal lattice produces freestanding wires with triangular cross sections.[52,119] Figure 2 A shows steps for

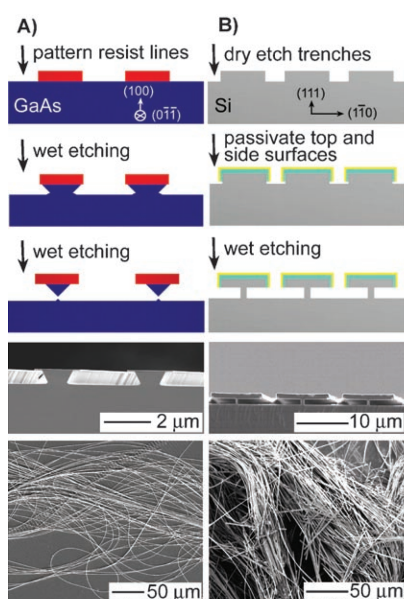

Figure 2. Schematic illustration of the fabrication of micro- and nanoscale wires and ribbons of single-crystalline GaAs (A) and Si (B) by use of anisotropic wet-chemical etching techniques applied to bulk wafers of these materials. The bottom frames show scanning electron micrographs. The bottom two panels of figure 2B were adapted from reference [120].

generating triangular wires from GaAs wafers. The top frame shows lines of resist patterned along the $(0\bar{1}\bar{1})$ direction on the GaAs (100) surface. The second frame shows the resulting profiles after wet etching in a phosphoric acid hydrogen peroxide solution according to the mechanism given in Equation (5).

$$GaAs + H_3PO_4 + 4\,H_2O_2 \rightarrow GaPO_4 + H_3AsO_4 + 4\,H_2O \qquad (5)$$

This reaction includes chemical oxidation of GaAs by hydrogen peroxide followed by removal of the oxidized products by phosphoric acid. Completing the etching process and then removing the resist produces freestanding GaAs wires. The fourth frame in Figure 2 A shows partially undercut GaAs wires, and the bottom frame shows fully undercut GaAs wires randomly assembled on the mother wafer, which demonstrates their mechanically flexible nature,[52,119] consistent with the discussion in Section 2.

A different but conceptually related approach can generate single-crystal silicon ribbons, platelets, and bars from bulk silicon (111) wafers.[50,120,121] Figure 2B depicts the fabrication sequence. For ribbons with rectangular profiles, the process begins with the patterning of lines of resist perpendicular to the Si $(1\bar{1}0)$ planes and then etching trenches into the exposed silicon (top frame of Figure 2B). Depositing SiO_2 (≈ 60 nm) followed by Si_3N_4 (≈ 300 nm) forms a resist bilayer on all of the silicon surfaces. Depositing titanium (3 nm) and gold (50 nm) metal by electron-beam evaporation at an oblique angle to the wafer surface and then removing the unprotected SiO_2/Si_3N_4 exposes the silicon planes (i.e. Si $(1\bar{1}0)$) as shown in the second frame in Figure 2B. For the silicon etchant KOH, this group of planes etches quickly in comparison to the other silicon planes, according to the overall redox reaction (6).[122]

$$Si + 2\,H_2O \rightarrow SiO_2 + 2\,H_{2(g)} \qquad (6)$$

In this process, the silicon surface is oxidized by OH^- ions, thus consuming water molecules and releasing hydrogen in the process. A major drawback of KOH is that it can introduce mobile ions that are detrimental to electronic applications.[123] As a result, etchants such as tetramethylammonium hydroxide (TMAOH) that are CMOS compatible are preferred.[120,123] The etching chemistry for TMAOH is similar to that in Equation (6) although TMAOH exhibits lower etch rates and different surface morphologies depending on the wafer orientation.[124]

In either case, the Si $(1\bar{1}0)$ etch fronts proceed in a horizontal fashion until they meet to complete the undercut and release freestanding single-crystal silicon micro- and nanostructures with rectangular cross sections (third frame in Figure 2B). The fourth frame in Figure 2B shows 500 nm thick, 200 µm long, and 7 µm wide silicon ribbons; the final frame depicts ultralong (up to 6 cm) silicon ribbons. These images illustrate the smooth surface morphologies and good mechanical flexibility of ribbons produced by this approach. By carefully controlling the processing parameters, ribbons, platelets, and bars with dimensions between 100 nm and the size of the wafers (thickness and diameters) can be formed in flexible and stretchable configurations.[120] Similar strategies can produce large quantities of such elements either by repeated application of procedures like those outlined above or by other techniques. One such technique relies on sculpted ripple patterns on the sidewalls of the vertical trenches formed in the first etching step as presented in Figure 3 A and B. These patterns can be produced by controlling the etching sequence in an inductively coupled plasma reactive ion etching (ICPRIE) system.[121] The ripples yield shadows during an angled metal evaporation step such that etching after this evaporation creates multilayer stacks of semiconducting nanoribbons (Figure 3C and D). Figure 3E shows the generation of relatively large amounts (e.g. milligram quantities) of material fabricated in this way.[121]

The types of top-down approaches described in this section can, of course, be used with materials other than

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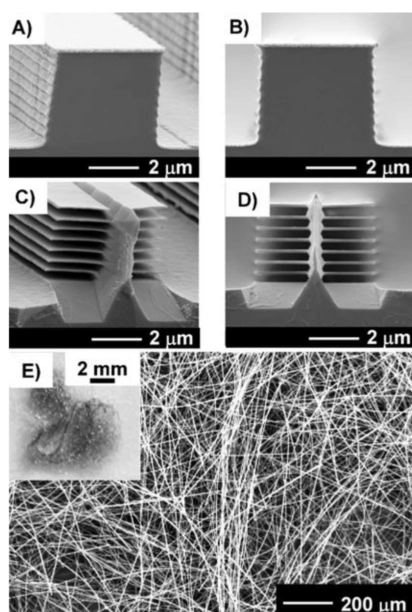

Figure 3. Angled (A and C) and cross-sectional (B and D) scanning electron micrographs of multilayered structures of silicon before (A and B) and after (C and D) etching with KOH. Completing this etch lifts off from the wafer bulk quantities of single-crystalline silicon ribbons (E). Reproduced with permission from reference [121] copyright American Chemical Society.

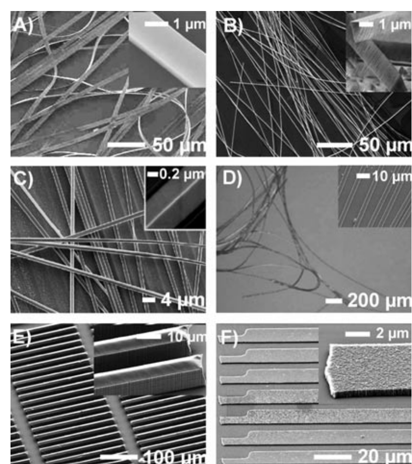

Figure 4. Scanning electron micrographs of microstructured semiconductor (μs-sc) elements. μs-Si (A, reproduced with permission from reference [51] copyright American Institute of Physics), μs-GaAs (B), μs-InP (C, reproduced from reference [119]), μs-GaN (D, reproduced from reference [125]), thick μs-Si (E, adapted from reference [120]), and μs-diamond (F).

GaAs and Si. Figure 4 shows, in addition to these two materials, examples of structures of InP (Figure 4C),[52,119] GaN (Figure 4D),[125] thick silicon bars (Figure 4E),[120] and diamond (Figure 4F).[126] These micro- and nanostructures exhibit good surface uniformity, morphologies and materials quality, and their geometries can be easily controlled. The main limitations of this top-down approach include: 1) compositions are limited to materials that are readily available in wafer or thin-film forms, 2) finite surface roughness associated with the etching processes, and 3) minimum lateral dimensions that are larger than about 10 nm, due to practical limitations in the lithography and etching.

4. Assembly of Micro- and Nanoscale Semiconductor Elements

A challenge for integrating elements formed either by "bottom-up" or "top-down" techniques into macroelectronics is in guiding their assembly into well-defined and useful layouts. The ideal configuration often involves perfect alignment and uniform end-to-end registration, in horizontal arrays at specified locations across a device substrate. The following sections describe some strategies for achieving assemblies that have some of these characteristics.

4.1. Guided Self-Assembly

Often, micro- and nanostructures generated by bottom-up approaches exist either as random networks dispersed in solution or on a surface, or as vertically aligned arrays; neither layout can be easily integrated into conventional electronic device layouts. The use of external forces such as those associated with microfluidic shear flows, surface compression (i.e. Langmuir–Blodgett), and electric or magnetic fields can be employed to assemble solution-based nanowires/ribbons into ordered arrays.[127–131]

In addition to these fluidic based approaches, two relatively recent methods for large-area integration have been introduced.[132,133] The first[132] relies on a mechanical process followed by a dry transfer printing method to assembly well-aligned films of nanowires onto a receiving substrate. In this case, the nanowires are synthesized by nanoparticle-directed growth on a mother substrate which is subsequently placed into contact with a receiving substrate patterned with a spacer (i.e. photoresist layer) that defines the nanowire layout. Applying pressure (i.e. shear force) and removing the mother substrate leaves well-aligned arrays of nanowires for subsequent device applications.[132] The second method involves expanding a polymer suspension of wires into a balloon shape.[133] The deformations that occur in the polymer during the expansion rotate the wires into aligned arrays. These wires can be transferred from these balloons to other substrates.[133]

Although these methods show some promise, further development will be required for implementation at high speeds, over large areas, and with the level of control and uniformity needed for applications in electronics. For example, in most of the methods described above, the aligned arrays exhibit poor end-to-end registry, and the distances between adjacent wires is not well controlled. Also, the use of solvents or surfactants or polymers that are not already established for use electronics could represent a disadvantage.

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4.2. Dry Transfer

Deterministic, dry transfer of micro- and nanoscale semiconductor elements provides an alternative integration strategy.[49–52,57–59,102,119–121,125,134–143] This approach uses a rubber stamp produced by the methods of soft lithography[144] to retrieve elements from a source substrate and deliver them to a flexible device substrate.[42,49–51,57–59,102,119–121,125,134–143] In contrast to the probabilistic mechanisms that occur during assembly methods of the type described in the previous section, transfer printing maintains mechanical contact to the semiconductor structures throughout the transfer process and is therefore deterministic. As a result, transfer printing is capable of extremely high transfer yields, with only minimal levels of positional/orientational disorder introduced during the process. When used in conjunction with semiconductor structures produced by the top-down approaches described previously or well-ordered arrays created by bottom-up synthesis, transfer printing can deliver near-perfect semiconductor arrays to virtually any kind of substrate. The discussion below focuses on µs-sc elements.

Figure 5 describes the transfer printing process. To begin, a polydimethylsiloxane (PDMS) rubber stamp contacts the µs-sc structures on a "mother" substrate. The stamp may contact all such elements on the substrate surface (e.g. using a flat stamp) or only a selected fraction of them determined by the relief features of the stamp.[137] The stamp and the contacted µs-sc then separate from the mother substrate and contact a new substrate (i.e. receiving- or target-substrate) of virtually any form and composition. Removal of the stamp from the receiving substrate transfers the µs-sc elements and completes the process.

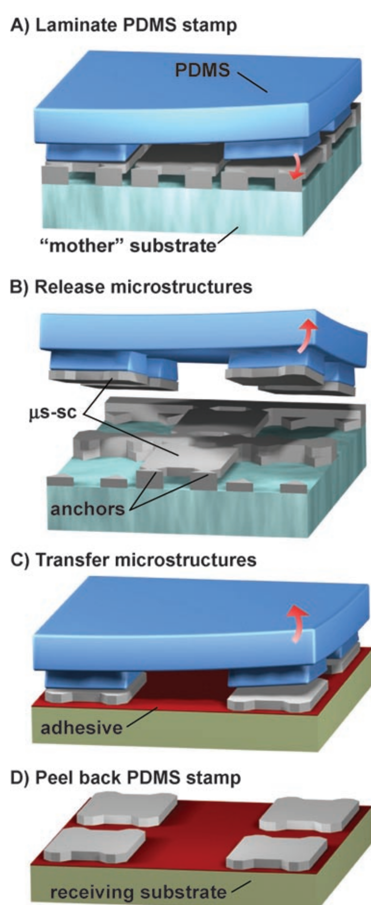

Figure 5. Schematic illustration of a transfer approach that uses a rubber stamp to remove selected collections of semiconductor micro- and nanostructures from a wafer and to deliver them to a receiving substrate.

High-fidelity transfer requires knowledge and careful control of the physical processes that direct the transfer of µs-sc elements from a substrate to a stamp and vice-versa. Chemical, geometrical, and kinetic considerations play important roles in guiding the direction of transfer, that is, the preferential adhesion of µs-sc elements to a stamp during retrieval from a mother substrate and the preferential adhesion to a target substrate during printing. Typically, the interfacial interaction between the PDMS stamp and µs-sc structures is dominated by Van der Waals (VdW) forces,[145–147] but manipulating the surface chemistry of the stamp can strengthen the adhesion of the µs-sc, even to the extent of strong bonding for applications in which the PDMS substrate is used for stretchable electronics (see Section 6). PDMS is composed of 3D cross-linked structures with repeating units of -$(CH_3)_2SiO_2$-. The pristine PDMS surface is usually covered with a high density of methyl groups (-CH_3), which leads to hydrophobicity.[148] Oxidizing the PDMS surface by exposure to highly active oxygen species, such as O_2^+, O_2^-, O generated from oxygen plasma, and ozone generated by UV irradiation or other means, leads to a PDMS surface that will react with a wide range of materials such as ceramics and oxides, to form strong chemical bonds, simply upon physical contact at room or slightly elevated temperatures.[52,57,119,143,149] The enhanced reactivity is attributed to the conversion of the hydrophobic surface to a strongly hydrophilic state due to the formation of surface silanol groups (-Si-OH).[149,150] This chemistry provides a means to create adhesion of variable strength, controlled by the fractional coverage of silanol groups, between the stamp and µs-sc elements that bear appropriate surface chemistries.[52,139]

In the case of printing, the extent of stamp oxidation must be carefully controlled so that the stamp/µs-sc interface can be readily broken during the printing step.[52,139] Fortunately, VdW forces from untreated PDMS stamps are usually sufficient for retrieval of µs-sc elements, especially when the retrieval is performed at high separation speeds. The strength of adhesion between PDMS and the µs-sc is strongly rate-dependent due to the viscoelastic properties of PDMS.[102,151] At low speeds, the energy required to separate PDMS from a rigid body is relatively low, due to the low surface energy ($\approx 20\ mJ\,m^{-2}$) of PDMS.[152] At higher speeds, however, the energy required to separate the two is much greater, and as a result, fast removal of a stamp from a mother substrate can lead to improvements in the yield of retrieving the µs-sc. Further improvements in retrieval yields come through careful design of the structures themselves.[138] For the case of structures formed by "top-down" procedures, before retrieval, the µs-sc elements are typically freestanding, but often left partially connected through anchoring elements to

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the mother substrate to maintain their lithographically defined organization even after complete undercut etching. During retrieval, the structures must separate from the anchors by fracture. This separation process can be improved, for example, by the introduction of stress concentration centers that facilitate fracture and improve retrieval yields.[138]

During the printing step, the previously mentioned condensation reactions and other chemical reactions[153] may be employed to produce strong adhesion between the µs-sc and the target substrate. Other notable interfacial interactions that are useful for producing this adhesion are the interaction of thiol groups with noble metals or III–V semiconductors[153–155] and cold-welding between contacted metal thin films.[155–159] The viscoelastic/kinetic effects described in the previous paragraph lead to improvements in printing reliability by slow separation of the stamp from the target substrate.[102,160] In addition to interfacial chemistry and kinetic effects, another critical consideration during printing is that the µs-sc should make full, conformal contact with at least some region of the receiving substrate. During retrieval, the low modulus of the PDMS elastomer facilitates conformal contact to the µs-sc elements, but during printing this kind of contact can be achieved by shape complimentarily or by the use of conformable adhesive layers on the target substrate. One important and simple example of shape complimentarity is the contact of smooth surfaces (few nanometer-scale roughness or better) of µs-sc elements to the smooth surface of a target substrate. In these instances, the µs-sc structures transfer to the substrate easily through nonspecific surface interactions, including VdW, in processes analogous to direct wafer bonding.[102,161,162] Figure 6 shows several examples of such printed systems. Figure 6A and B show images of Si-III–V heterogeneous integration by printing. Figure 6A shows µs-GaN bars ($2\times5\times180\ \mu m^3$) printed directly onto Si (100) and Figure 6B shows µs-Si ribbons ($3\times25\times250\ \mu m^3$) printed directly onto a GaAs wafer.[102] This kind of "adhesiveless" transfer printing can even deliver µs-sc elements to curved surfaces, as seen in Figure 6C and D, by rolling a cylindrical substrate across or pressing a spherical substrate into a soft stamp that supports smooth silicon microstructures.[102] Transfer to structured surfaces is also possible as long as some significant fraction of the printable structures makes conformal contact to the substrate, as in the adhesivelessly printed silicon woodpile structure shown in Figure 6E. When shape complimentarily is lacking, or when one or more of the interfaces is not sufficiently smooth to produce significant adhesion, thin film adhesive layers can help guide transfer. These soft, typically polymeric, materials ensure complete conformal contact between µs-sc elements and the target substrate and can improve printing yields dramatically. Often the stamp and printable structures contact these materials when they are flowable, in the uncured or partially cured state. While the stamp is still in contact, exposure to light, heat, or some combination cures these adhesive materials, strongly binding the µs-sc elements to them. Several examples of thin film adhesives for this kind of transfer printing include polyimide,[134,136] polyurethane,[52,119,137] benzocyclobutene-containing siloxane polymers (BCB),[163] PDMS,[120] and epoxy resins.[42,50,142] Figure 6F–H show some examples of printed systems that use thin film adhesives: µs-Si ribbons on a PDMS film on a glass rod (Figure 6F), and µs-InP (Figure 6G) and µs-GaAs (Figure 6H) wires on a polyurethane film on PET.[52,119]

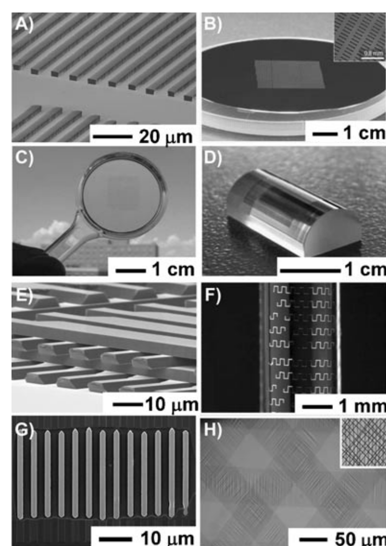

Figure 6. Images of inorganic single-crystalline wires and bars printed onto various types of substrates. µs-GaN bars on a Si (100) wafer (A); µs-Si ribbons on a GaAs wafer (B); µs-Si elements on a spherical polycarbonate lens (C) and on a cylindrical glass lens (D); multilayer stacks of µs-Si bars (E); µs-Si ribbons on a glass rod (F); µs-InP (G) and µs-GaAs (H) wires on a thin plastic substrate. The cases (A–E) used adhesiveless printing by kinetic control; (F–H) used thin polymer film adhesives to guide the transfer. Panels A–D reproduced from reference [102] copyright Nature Publishing Group. Panels G and H were reprinted with permission from reference [52] copyright American Chemical Society.

In its simplest implementations, this kind of transfer printing may be performed manually. Greater control may be accomplished, however, with the use of a mechanical printing tool (Figure 7). Such a tool comprises *x*-, *y*-, and *z*-axis linear stages, and tilt- and rotation stages to manipulate a stamp relative to the source and target substrates at reproducible and controllable speeds. Load cells and integrated optics monitor the alignment and the forces of contact between the stamp and substrate. When equipped with a composite stamp (a thin elastomer layer backed with a high-modulus material) to avoid distortions,[164–166] the tool in Figure 7 can achieve $\approx 2\ \mu m$ registration across a stamp–substrate contact region several centimeters across and can handle substrates as large as 400 mm. This tool and others like it but designed for conventional soft lithography or nanoimprinting[164,167] represent important technological steps toward machines that may someday perform transfer printing and other soft-lithographic techniques with high throughput in industrial settings. Such printers, equipped with molded stamps, contact and retrieve a selected fraction of µs-sc elements from a densely packed array on a mother substrate and transfer them to a larger plastic substrate. The printer then returns to repeat the process with the remaining µs-sc elements on the mother substrate, producing a sparse array on the plastic substrate in a process called "selective transfer" or "area multiplication"

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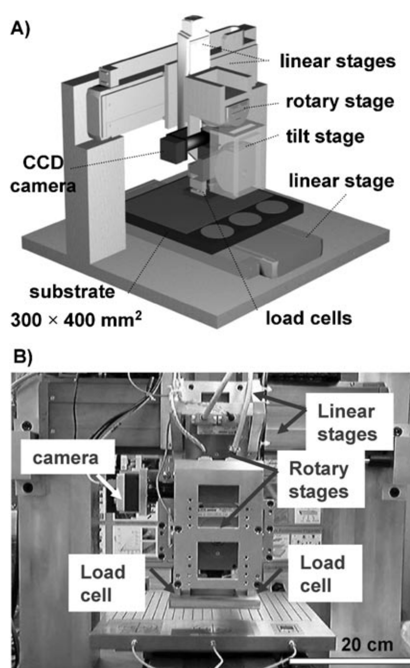

Figure 7. Schematic illustration (A) and a photograph (B) of an automated tool used to print μs-sc.

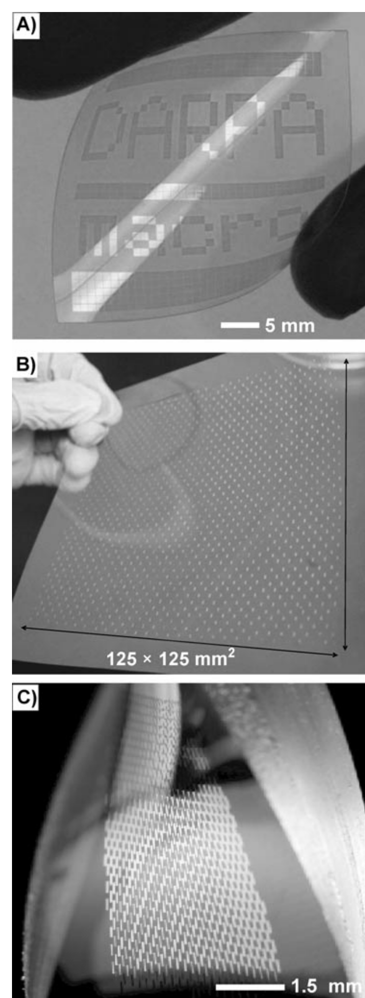

Figure 8. μs-Si on plastic (A, B) and rubber (C) substrates. Panel B was reproduced with permission from reference [137]

for large-area, flexible electronics.[120,137] Figure 8A and B shows two examples of sparse arrays of μs-Si ribbons transferred to a flexible PET substrate using photocurable polyurethane adhesive thin films, suggesting the ability to scale this transfer printing approach to substantial sizes,[137] whereas Figure 8C illustrates the ability to transfer silicon objects onto PDMS stamps that can stretched and compressed and incorporated into devices, as described in Section 6.

5. Applications in Flexible Electronics

5.1. Nanostructures Generated by Bottom-up Approaches

Semiconductor nanostructures formed by bottom-up approaches can enable the development of novel electronic and photonic devices and a host of other emerging applications.[168] The key attributes of this approach include the separation of processing steps that require high-temperatures (i.e. growth of nanowires, doping) and other low-temperature steps (i.e. nanowire assembly) required for device fabrication. Recent studies demonstrate that single and heterostructured nanowires can be assembled onto either rigid or flexible substrates under ambient conditions to create on-chip photonic devices such as light-emitting diodes, lasers, active waveguides, integrated electrooptic modulators, and sensors.[64,108,169–173]

Similar nanowires have been implemented in a variety of electronic applications. For example, logic gates (e.g. OR, AND, NOR) can be fabricated from solution-assembled silicon and GaN nanowires.[174] In these cases, the nanowires can represent both the active channel regions and the gate electrodes. In addition, by adopting a solution-directed alignment approach, films of aligned silicon nanowires can be generated on plastic substrates for the fabrication of high-performance thin-film transistors.[175] Owing to the single-crystal nature of these nanoscale building blocks, devices that exhibit high carrier mobilities and transconductances can be achieved. Also, single nanowire transistor devices suggest per-wire mobilities as high as 365 $cm^2 V^{-1} s^{-1}$ can be achieved by flexible plastic substrates, with good mechanical stability, as indicated by only a fractional change in their electrical properties when bent to a radius of curvature of about 0.3 cm on a substrate of poly(ethylene terephthalate) with a thickness of 100 μm.[176] Circuit demonstrations including three-stage ring oscillators with frequencies of about 12 MHz at voltages of about 40 V have been achieved with aligned arrays of Si nanowires on glass substrates.[177]

Core–shell nanowires composed of Ge, Si and other materials can achieve improved performance capabilities.[178] Well-aligned arrays of GeSi nanowires can be created by the mechanical approaches described previously.[132] Such arrays

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can be used as effective semiconductor thin film materials for field-effect transistors, which are capable of integration in two- or three-dimensional stacked layouts with up to 10, or more, layers.[132] In addition to electronics, similar arrays can be implemented in sensors for label-free detection of biological and chemical species.[179–183]

5.2. Nanostructures Generated by Top-down Approaches

The structures highlighted in Section 3.2 can be used to form high-performance transistors and other electronic devices. As examples, Figure 9 shows Si MOSFETs on a thin (≈ 25 μm) polyimide (PI; Kapton) sheet, and GaAs MESFETs, and GaN HEMTs on PET (180 mm) substrates, by use of μs-Si ribbons ($W = 87$ μm, $L = 250$ μm, and thickness = 290 nm), μs-GaAs wires ($W = 2.1$ μm, $L = 250$ μm , and thickness = 2.1 μm) and μs-GaN bars ($W = 10$ μm, $L =$ 150 μm, and thickness = 1.2 μm), respectively. In each case, high-temperature processes needed for the contacts (i.e. the source/drain doping for the MOSFETs and the ohmic contact formation for the MESFETs and HEMTs) were performed on the wafers from which the μs-sc elements were produced, thereby avoiding the need for high-temperature processing on the plastic substrates. The other device fabrication steps (i.e. gate dielectric deposition for the MOSFETs and Schottky contacts for the MESFETs and HEMTs) were performed directly on the plastic after dry transfer printing of the preprocessed semiconductor elements. Effective channel mobilities of the μs-Si MOSFETs can be extracted from measurements of the variations in drain/source current (I_{DS}) with gate voltage (V_{GS}). These values, which are between 500 and 600 $cm^2 V^{-1} s^{-1}$ in the linear regime and about 500 $cm^2 V^{-1} s^{-1}$ in the saturation regime, approach those in similar devices produced on SOI wafers, and are superior to laser-annealed polycrystalline silicon devices on plastic substrates.[136] These good performance characteristics enable high-frequency operation. The unity-current gain frequencies, f_T, measured in common-source configuration, for μS-Si MOSFETs and μS-GaAs MESFETs on plastic, are about 500 MHz for the μS-Si MOSFETs[136] and about 1.5 GHz[141] for the μS-GaAs MESFETs for relatively long-channel ($L_c >$ 2 μm) devices with simple designs. Improved device designs enable f_T in the GHz range.[184] These results illustrate that the frequency responses of TFTs based on μs-sc elements on plastic substrates can be comparable to those found in conventional wafer-based systems.[184]

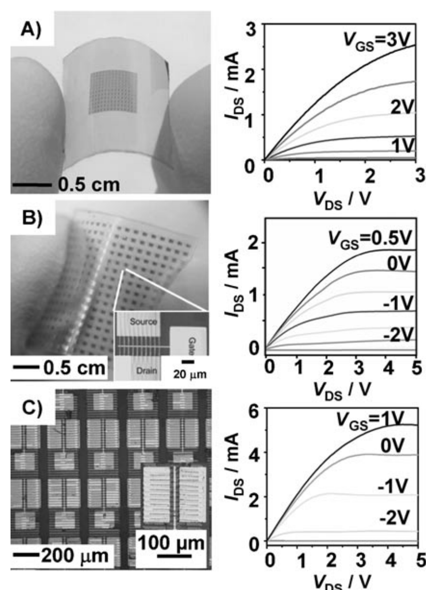

Figure 9. Images and current–voltage characteristics of field-effect transistors: μs-Si ribbon based MOSFETs (A, Reproduced with permission from reference [136] copyright IEEE); μs-GaAs wire-based MESFETs (B, adapted with permission from reference [141] and reference [190] copyright American Institute of Physics); μs-GaN ribbon-based HEMTs (C). I_{DS} is the current that flows from the source to the drain electrodes; V_{DS} is the potential difference between these two electrodes; V_{GS} is the gate voltage.

Multiple devices of this type can be combined to produce integrated circuits. Figure 10 illustrates various analog and digital examples that use μS-Si MOSFETs and μS-GaAs

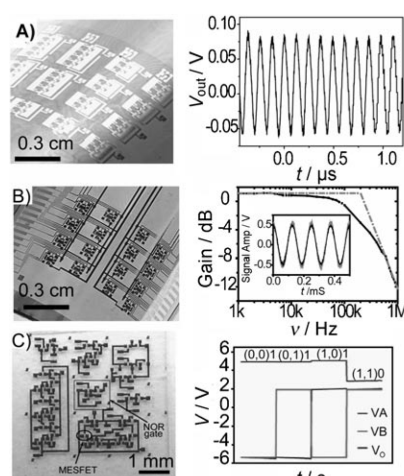

Figure 10. Simple electronic circuits built using printed μs-sc on plastic substrates. Five-stage ring oscillator based on μs-Si ribbons (A); differential amplifier based on μs-Si ribbons (B); NOR gates based on μs-GaAs wires (C, adapted from reference [140]). Panels A and B were adapted with permission from reference [135] copyright American Institute of Physics.

MESFETs. Figure 10 A shows an image and electrical measurements of a ring oscillator that consists of five NMOS inverters, also on PI. The oscillator exhibits a frequency of about 8 MHz, corresponding to a stage delay of 12 ns at a supply voltage, $V_{DD} = 4$ V. The operating voltages are much lower than those reported for ring oscillators fabricated by using polycrystalline Si on flexible substrates or by using nanowire transistors on rigid glass substrates, suggesting advantages for low power logic applications.[20,30,177,185] Figure 10 B shows an image and performance characteristics of a differential amplifier on a PI sheet. The circuit consists of a current source, a current mirror, a differential pair, and load to yield voltage gains of about 1.3 for a 0.5 V peak-to-peak (PP) input signal. Figure 10 C shows the integration of μs-GaAs MESFETs to form a NOR gate.[140] One MESFET

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(top) serves as the load and two identical ones in parallel (bottom) serve as switching transistors. Further integration of logic gates of this type and/or other passive elements (e.g., resistors, capacitors, inductors) offers the promise for high-speed, large-area electronic systems on plastic.

By electrically interconnecting NMOS TFTs with PMOS TFTs from μs-Si ribbons, low-power and high-performance complementary metal-oxide semiconductor (CMOS) logic structures on flexible plastic substrate can be achieved. Figure 11 A shows transfer curves for *p*-channel devices whose channel lengths (L_c) are between 2 μm and 24 μm, contact overlaps (L_o) between 1.5 μm and 5.5 μm, and channel widths (W) 180 μm.[186] The inset in Figure 11 A corresponds to typical characteristics for a device of $L_c =$ 9 μm. The on/off ratios, linear effective mobilities, and threshold voltages are about 10^6, $(200\pm20)\,cm^2V^{-1}s^{-1}$ and (-2.5 ± 0.5) V, respectively. Figure 11 B presents a CMOS inverter on a flexible plastic substrate, whose voltage transfer characteristics, optical image and circuit diagram and in its insets. The sharpness of voltage transfer is reflected in high gains (up to ≈ 150) and large sums of noise margins (high noise margin and low noise margin) of about 4.7 V at a supply voltage of 5 V.[186]

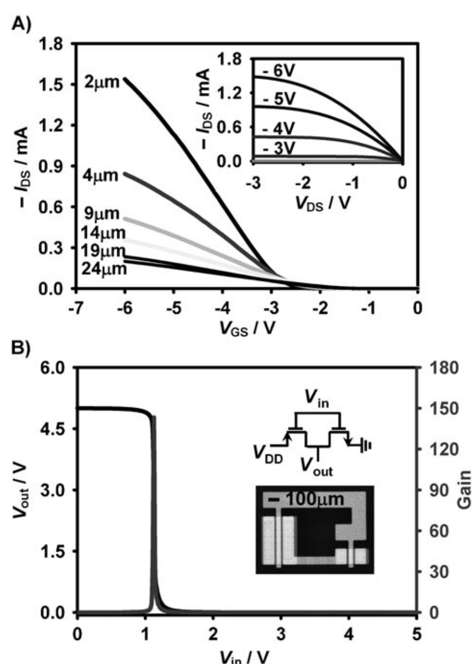

Figure 11. Current–voltage characteristics of PMOS transistors (A) and CMOS inverters (B) on plastic substrates. The inset in (A) shows the current voltage characteristics of a PMOS transistor with gate voltages varying from −3 to −6 V. The inset in (B) provides a circuit diagram and an optical micrograph. Reproduced with permission from reference [186] copyright IEEE.

6. Heterogeneous Integration

The same μs-sc/printing approach to flexible electronics enables the combined use of dissimilar classes of semiconductors to yield heterogeneously integrated systems, in ways that could be important for applications such as microfluidic devices with integrated electronics, chemical and biological sensor systems that incorporate unusual materials with conventional silicon-based electronics, and photonic and optoelectronic systems of semiconductors such as GaAs and GaN with silicon drive electronics. The process involves simply the repeated application of the printing and device fabrication steps described previously, but where the μs-sc elements for different devices come from different mother substrates.[134] The resulting circuits can involve either two-dimensional or three-dimensional multilayered layouts. In the latter case, after the first layer of devices is printed, the substrate is coated with a thin layer of polymer, which planarizes the first layer, and forms an insulating adhesive layer for the next level of devices. Since this interlayer polymer can be thin, vias can be easily etched into it, allowing interconnections between devices in different layers.[134] Figure 12 A shows a top view optical micrograph of a three-layer stack of μs-Si MOSFETs formed in this manner on a PI substrate, where the interlayer polymer is also PI. A 90° rotation of the device geometry for the second layer, relative to the first and third, helps to clarify the layout of the system. Figure 12 B illustrates schematic cross-sectional and angled views of the stacked structure. Figure 12 C presents top and angled views obtained by using a confocal optical microscope. Figure 12 D shows a large-area image of the 3D stack-arrayed μs-Si MOSFETs that use ribbons with $W = 87$ μm, $L =$ 250 μm, and thickness = 290 nm. Devices on each of the three layers show excellent properties (linear mobilities of $(470\pm30)\,cm^2V^{-1}s^{-1}$, on/off ratios $> 10^4$ and threshold voltages of (-0.1 ± 0.2) V) with no systematic differences between devices in different layers.

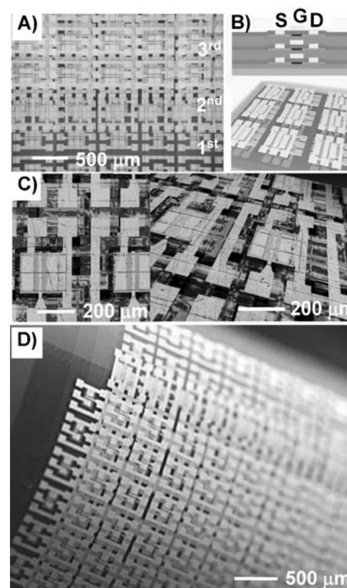

Figure 12. Schematic illustrations and images of trilayer stacks of μs-Si transistors, formed on plastic substrates by repetitive application of transfer printing. Top view optical image (A) and angled and cross-sectional schematic illustrations (B). Confocal top and angled views (C) and an image of the system bent around a cylindrical support (D). Reproduced with permission from reference [136] copyright AAS.

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Figure 13 shows a similar example, but here the different layers support different types of devices, in this case µs-GaN HEMTs ($W = 10$ µm, $L = 150$ µm, and thickness = 1.2 µm), single-walled carbon nanotube (SWNT) thin film transistors (TFTs, average tube diameters and lengths of ≈1.5 nm and ≈10 µm, respectively), and µs-Si- MOSFETs.[134] Figure 13 A and B show high-magnification optical and confocal images of the resulting array of devices, respectively. The µs-GaN HEMTs use the same design as those shown in Figure 9 C. The SWNT TFTs on the second layer use SiO_2 and an epoxy resin for the gate dielectric and Cr/Au for the source, drain and gate. The µs-Si MOSFETs have the same design as those shown in Figure 12. The devices exhibit similar characteristics to those fabricated on the mother wafers (Figure 13 C): Silicon MOSFETs have $V_{th} = (0.2 \pm 0.3)$ V, on/off ratios of more than 10^4, and linear mobilities of (500 ± 30) $cm^2 V^{-1} s^{-1}$; SWNT TFTs have $V_{th} = (-5.3 \pm 1.5)$ V, on/off ratios of more than 10^5, and linear mobilities of (5.9 ± 2.0) $cm^2 V^{-1} s^{-1}$; the HEMTs (bottom frame of Figure 13 C) have threshold voltages (V_{th}) of (-2.4 ± 0.2) V, on/off ratios of more than 10^6, and transconductances of (0.6 ± 0.5) mS. As with the simpler (i.e. single layer) single material systems, applications of these layouts in flexible electronics require good behavior under bending. Figure 13 D presents some optical images of the type of bending test in which we evaluated the flexibility for each type of systems composed of three-layer stacks of µs-Si, µs-GaN, and SWNT by performing frontward and backward bending tests. The effective transconductances of these devices (normalized to the transconductance in the unbent state) show no major changes to a bending radius of 3.7 mm. The total thickness of these multilayer devices, including the substrate, is less than 30 µm (device layers have a cumulative thickness of 1.7 µm, the PI interlayers have a cumulative thickness of ca. 1.5 µm, and the PI substrate has a thickness of 25 µm).

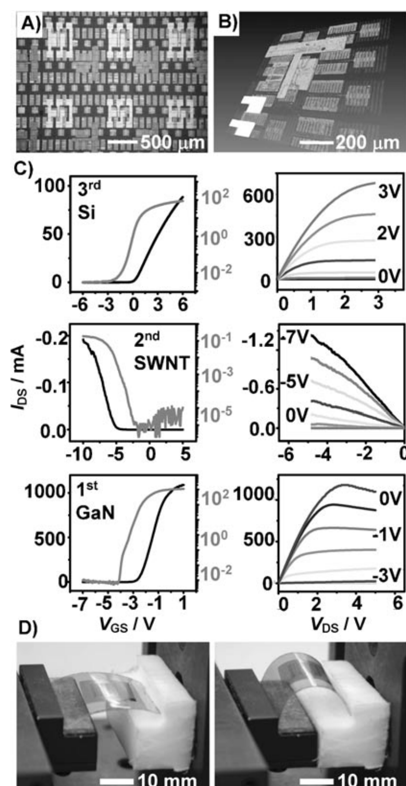

Figure 13. Images of a printed array of three-dimensional, heterogeneously integrated electronic devices that use µs-Si, µs-GaN, and single-walled carbon nanotubes printed on a polyimide substrate collected with a conventional optical microscope (A) and a scanning confocal microscope (B). Electrical characteristics of devices in the different layers (C). Bending fatigue testing of three-layer stacks of µs-Si, µs-GaN, and SWNT transistors on a thin plastic sheet. Images of the testing apparatus and a device under test at small (left frame) and moderate (right frame) degrees of bending (D). Reproduced with permission from reference [136] copyright AAS.

7. Applications in Stretchable Electronics

Mechanical flexibility is a useful characteristic that can be achieved with thin devices and substrates, and/or clever engineering approaches such as neutral mechanical plane designs. Stretchability is possible with thin, "wavy" structures that behave mechanically similar to an accordion bellows which when integrated on PDMS substrates yields system-level stretchability, even with semiconductor materials that are intrinsically brittle. The amplitudes and wavelengths change to accommodate strains applied to the PDMS.

Figure 14 outlines the process for fabricating such systems. The process starts with the generation of µs-sc ribbons using

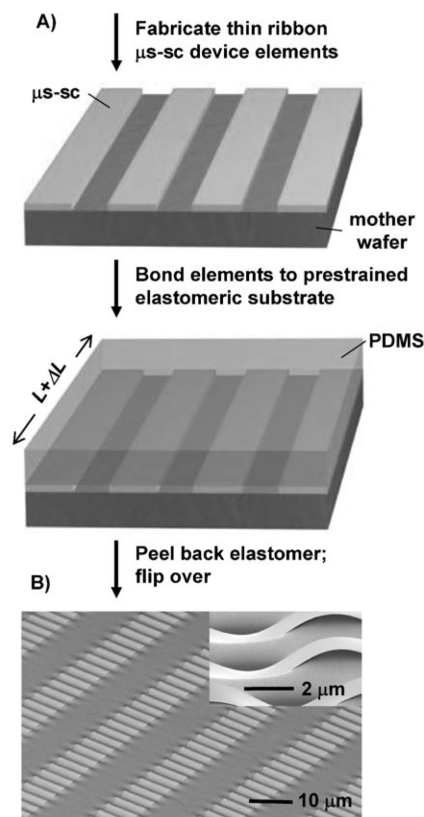

Figure 14. A) Schematic illustration of the steps involved in fabricating "wavy" µs-sc ribbons. B) Low and high (inset) scanning electron microscope images of wavy µs-Si ribbons on PDMS

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"top-down" approaches. Next, laminating a pre-strained (ε_{pre}) PDMS substrate against ribbons oriented along ε_{pre}, leads to the formation of conformal contact and bonding between the ribbons and PDMS. Peeling back the PDMS transfers all the ribbons to the surface of the PDMS. Relaxing ε_{pre} leads to compressive stresses that induce nonlinear buckling instabilities in the ribbons to produce sinusoidal, wavy geometries as depicted in the bottom frame of Figure 14B.[57,59,187] Figure 14B shows images of structures formed with µs-Si (thicknesses ca. 100 nm, widths ca. 20 µm) ribbons using a prestrain of 3%. Close inspection (inset of Figure 14B) of the interface between the PDMS and the ribbons at the raised regions reveals intimate contact between the PDMS and the ribbons. The level of prestrain, the mechanical properties of the PDMS and Si, the widths, lengths, and thicknesses of the ribbons determine the amplitudes and wavelengths of these structures. The same procedures can be applied to µs-sc other than silicon by, for example, coating their surfaces with SiO_2 or other layers that can react with the oxidized surface of the PDMS. In all cases, suitable reaction conditions can produce bonding that is sufficiently strong to remove the µs-sc from the PDMS and to yield an integrated system with mechanical failure modes that are cohesive in the PDMS and the µs-sc rather than adhesive at the interface.

AFM data of wavy structures fabricated following the procedure shown in Figure 14 confirm that the wavy profiles are purely sinusoidal.[57] This observation, as well as the extracted amplitudes and wavelengths, agree with theoretical calculations that include finite deformations and geometrical nonlinearities.[188] In particular, these models predict a vertical displacement (y_{wavy}) that depends on position (x) along the ribbons according to Equations (7)–(13),

$$y_{wavy} = A_{wavy}\sin\left(\frac{2\pi}{\lambda_{wavy}}x\right) \quad (7)$$

$$\lambda_{wavy} = \frac{\lambda_0}{(1+\varepsilon_{pre})(1+\xi)^{1/3}} \quad (8)$$

$$A_{wavy} = \frac{A_0}{\sqrt{1+\varepsilon_{pre}}(1+\xi)^{1/3}} \quad (9)$$

$$\lambda_0 = \frac{\pi h}{\sqrt{\varepsilon_c}} \quad (10)$$

$$A_0 = h\sqrt{\frac{\varepsilon_{pre}}{\varepsilon_c}-1} \quad (11)$$

$$\xi = \frac{5\varepsilon_{pre}(1+\varepsilon_{pre})}{32} \quad (12)$$

$$\varepsilon_c = 0.52\left[\frac{E_{PDMS}(1-\nu^2_{ribbon})}{E_{ribbon}(1-\nu^2_{PDMS})}\right]^{2/3} \quad (13)$$

where ε_c is the critical strain for buckling, ε_{pre} is the prestrain, λ_{wavy} and A_{wavy} are the wavelength and amplitude of the resulting waves, respectively. The Poisson ratio is ν, the Young's modulus is E, the ribbon thickness is h, and the subscripts refer to properties of the ribbons or PDMS. The resulting physics is very similar to, but not exactly the same as, an accordion bellows, as described in Section 2.

Two-dimensional (2D) wavy geometries can be formed in µs-sc membranes using the fabrication strategy shown in Figure 14, but with PDMS substrates that are biaxially prestrained.[143] Here an SOI wafer provides the source of the membranes; small holes allow access of the HF undercut etchant to the buried oxide. Two-dimensional wavy membranes of this type can be stretched along any axis (Figure 15).

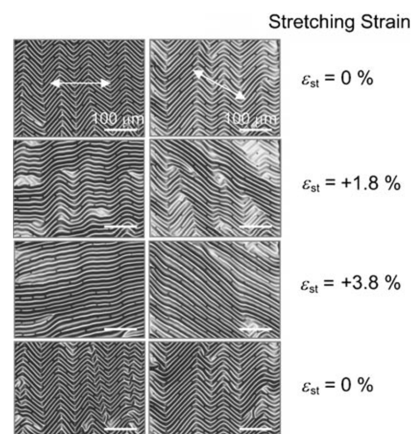

Figure 15. Optical micrographs of a wavy µs-Si nanomembrane under uniaxial strain for two different directions (indicated by arrows in the top frames). The images were taken in the unperturbed state before stretching (top frames), at uniaxial applied tensile strains of 1.8% (top middle frames) and 3.8% (bottom middle frames) the relaxed state after the stretching (bottom frames). Reproduced with permission from reference [143] copyright American Chemical Society.

These types of systems provide stretchability to levels of strain of 10–20%. While the ability to accommodate strains in this range is useful for some applications, more extreme levels of stretchability could be valuable. The essential limitation of the approaches described above is that the mechanics of the systems define the layouts of the wavy structures. These layouts are not optimized for stretchability. The ability to pattern adhesion sites, either by manipulating the surface chemistry of the PDMS or the µs-sc provides a route to avoid this limitation.[187] Figure 16A illustrates the process. Here, advanced soft lithographic techniques allow the PDMS substrates to be oxidized in patterned areas.[58,150] Adhesion to the µs-sc is possible only in these regions. Bonding and then relaxing the prestrain leads to buckled structures that involve complete separations of the ribbons from the PDMS in the unoxidized regions. Figure 16B shows buckled µs-GaAs ribbons (thicknesses ca. 270 nm covered with 30 nm SiO_2, widths ca. 100 µm) formed with a prestrain of 60% on a PDMS substrate with patterned regions of oxidation (surface activated) in the geometry of parallel stripes (widths, W_{act}, of 10 µm) separated by wide, unoxidized (inactivated) regions (widths, W_{in}, of 400 µm). Theoretical analysis[189] shows that vertical displacements associated with these buckles (measured relative to the flat surface of the PDMS stamp) can be written according to Equations (14)–(17)

$$y = {}^1\!/_2 A_{buckled}\left(1+\cos\frac{\pi}{L_1}x\right) \quad (14)$$

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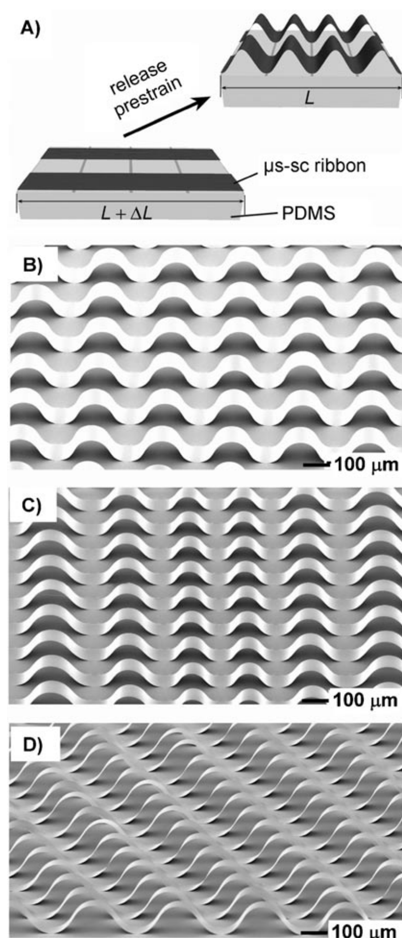

Figure 16. Schematic illustration of the formation of "buckled" µs-sc ribbons on an elastomeric substrate with lithographically patterned surface adhesion sites (A). Scanning electron micrographs of periodic structures with fixed phases of µs-GaAs (B), chirped µs-Si structures (C), and periodic µs-Si structures with spatially varying phases (D). Panels B–D were reprinted with permission from reference [58] copyright Nature Publishing Group.

$$A_{\mathrm{buckled}} = \frac{4}{\pi}\sqrt{L_1 L_2\left(\frac{h h \pi \pi}{12 L_1 L_1}\right)} \quad (15)$$

$$L_1 = \frac{W_{\mathrm{in}}}{2(1+\varepsilon_{\mathrm{pre}})} \quad (16)$$

$$L_2 = L_1 + \frac{W_{\mathrm{act}}}{2} \quad (17)$$

The buckle width of the initial buckles is $2L_1$ and the periodicity is $2L_2$. Because $hh\pi\pi/12L_1L_1$ is much smaller than $\varepsilon_{\mathrm{pre}}$ (i.e., >10% in most cases) for $h<1$ µm, the amplitude can be simplified as $(4/\pi)\sqrt{L_1 L_2 \varepsilon_{\mathrm{pre}}}$, which is independent of the properties of ribbons (e.g., thickness, chemical composition, Young's modulus, etc.). As a result, the geometries of buckles are mainly determined by the layout of the adhesion sites and the prestrains. The maximum tensile strain (i.e. peak strain) in the buckled ribbons shown in Figure 16B is only 0.61% according to Equation (18).

$$\varepsilon_{\mathrm{buckled}}^{\mathrm{peak}} = \frac{h}{4} A_{\mathrm{buckled}}\left(\frac{\pi}{L_1}\right)^2 \quad (18)$$

This value is about 100 times smaller than the $\varepsilon_{\mathrm{pre}}$. This mechanical advantage is significantly larger than that possible with the fully bonded geometries. Encapsulating these structures in PDMS by casting and curing enables reversible and robust behavior with applied strain.[58]

In addition to these relatively simple grating geometries, complex layouts such as chirped structures in which the widths and amplitudes of adjacent buckles vary in each of the ribbons (Figure 16C) and those with phases in the buckles that vary linearly with distance perpendicular to the lengths of the ribbon (Figure 16D) can also be fabricated. Multilayer structures that include µs-sc elements and other materials (e.g., metal layers for electrodes, dielectric layers, etc.) for functional devices are possible. Most conveniently, the processing for these other layers is accomplished on the mother wafer before transfer to the PDMS. For example, stretchable MOSFETs consisting of wavy µs-Si ribbons (thickness of 2.5 µm and width of 50 µm) with integrated metals electrodes, SiO_2 dielectrics, and doped contacts are possible.[57–59] Figure 17A shows images of such a device, collected at different levels of applied strain, that is, compressed by 9.9% (top frame) and stretched by 9.9% (bottom frame). The electrical properties do not change significantly (<20% in saturation current) when stretched or compressed up to about 10% (Figure 17B), and the device functions well even after hundreds of cycles of compressing/stretching, with mobilities of about 100 $cm^2 V^{-1} s^{-1}$.

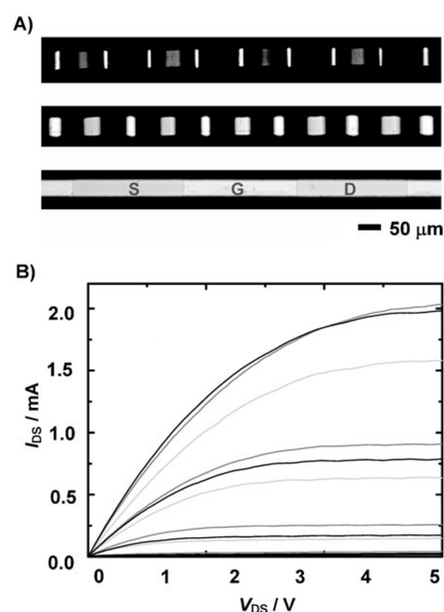

Figure 17. Optical images of a "wavy" µs-Si ribbon-based transistor on an elastomeric substrate in unstrained (top), compressed (middle), and stretched (bottom) states (A). Electrical characteristics of the device at different applied strains (B). The sets of curves correspond to devices measured under different strains (approximately −10, 10, and 0% for the top, middle, and bottom curves, respectively) at different gate voltages. Adapted with permission from reference [58] copyright The Royal Society of Chemistry.

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Figure 18 A shows a wavy μs-GaAs MESFETs under different applied strains. These MESFETs are formed by using μs-GaAs ribbons (thicknesses ca. 270 nm and widths ca. 100 μm) with integrated ohmic source and drain electrodes

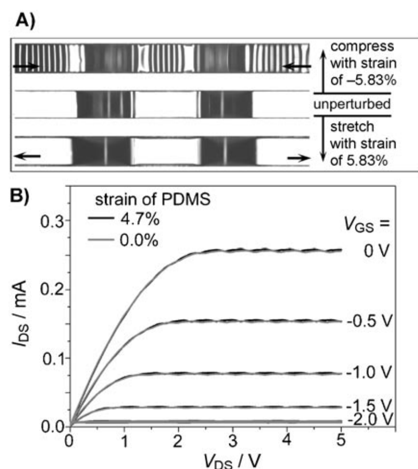

Figure 18. Optical images of a GaAs MESFET embedded in a PDMS matrix; unstrained (middle), stretched (by 5.83 %; bottom), and compressed (5.83 %; top) states (A). Current–voltage characteristics of a MESFET under different levels of stretching (B). Reproduced from reference [59].

(Ge (70 nm)/Ni (10 nm)/Au (70 nm)) and Schottky gate contacts (Cr (75 nm)/Au(75 nm)).[59] Here, only van der Waals interactions bond the devices to the PDMS substrate. This feature and the spatially dependent changes in flexural rigidity associated with the patterned metal electrodes cause the device to separate from the PDMS in the bare GaAs regions upon relaxation of the prestrain. These buckled devices can be embedded in PDMS and then stretched and compressed with strains up to about 6 % without breaking the ribbons (Figure 18 A). At large compressive strains, short period wavy structures form in the electrode regions. Figure 18 B shows the electrical characteristics of a device formed on a PDMS with $\varepsilon_{pre} = 4.7\,\%$, recorded at applied strains of 0.0 % and 4.7 %, respectively.

8. Summary and Outlook

This review describes how micro- and nanoscale structures of inorganic semiconductors can be formed into well-ordered geometries and integrated with flexible substrates to yield high-quality electronic devices of various types. This class of materials approach to macroelectronics can complement more widely examined methods that use organic semiconductors, laser-annealed silicon, and others. The design choices and materials diversity collectively provided by these technologies might open up new application possibilities in electronics that are difficult to address in other ways. The opportunity for heterogeneous integration, in 2D or 3D layouts, together with unusual mechanical characteristics, such as stretchability, represent capabilities of particular interest. Developing new chemistries and materials for these systems, further investigating the mechanics and reliability upon bending, flexing, and stretching, together with the design and implementation of printing systems for the assembly all appear to be promising areas for future research.

Abbreviations

CMOS	complementary metal oxide semicoductor
HEMT	high electron mobility transistor
MESFET	metal semiconductor field-effect transistor
μs-sc	microstructured semiconductor
MOSFET	metal oxide semiconductor field-effect transistor
PDMS	polydimethylsiloxane
PET	polyethylene terephthalate
PI	polyimide
SLS	solution–liquid–solid
SNAP	superlattice nanowire transfer
SOI	silicon on insulator
TFT	thin film transistor
VLS	vapor–liquid–solid

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